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DESIGN OF FREQUENCY MULTIPLIER BASED ON DOUBLE-EDGE COUNTER AND ITS ANALYSIS

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Abstract. *In recent years, clocks with various frequencies are needed to drive each system within mobile communication devices. The clock signal generator is required to have low power consumption, quick clock signal generation, clock pulse width, and stability. In this paper, we propose the digital frequency multiplier based on the double-edge counter. Since this circuit uses a double-edge counter to count the reference clock, the counting error can be less than half its period. As a result, the steady-state frequency error of the output signal relative to the frequency of the input signal can be reduced to 1/2 of that of conventional methods. In addition, a fast recovery from the circuit stop state is possible, and a multiplied output signal can be obtained from the second cycle after the input signal is applied. These characteristics are clarified by simulation using Velilog-HDL.*
Keywords: Frequency multiplier, Double-edge counter, Steady-state frequency error

1. **Introduction.** In recent years, technological innovation in mobile communication devices has progressed dramatically and is one of the key items supporting the Internet of Things (IoT) in the future. In these mobile communication devices, clocks with various frequencies are needed to drive each system as they become more sophisticated. Clock signal generators used for these purposes have an important role in the following aspects. In terms of power consumption, if the clock signal generator can be stopped during system standby, it is possible to reduce not only the power consumption associated with stopping the clock signal supply to the system, but also that associated with the clock signal generator. For this reason, the generation of a quick clock signal when the system returns is an important factor for the clock generator [1-4]. In terms of the pulse spacing of the clock signal, an increasing number of systems have recently been using both the rising and falling edges of the clock signal for signal processing, and in such cases, generating a clock with a duty ratio of 50% is an extremely important performance factor [5]. In terms of system stability, with the digitization of various systems, timing adjustment with clocks has a significant impact, so stable clock generation is desirable. In terms of versatility,

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the development of a clock generator for each system increases costs, so a clock generator with a wide frequency bandwidth is desirable.

A phase-locked loop (PLL) is a circuit widely used as a clock signal generator for them. A PLL is a circuit that generates an output signal locked to an input signal by phase control. With the digitization of each system, PLLs based on all-digital configurations (DPLL: Digital PLL) have been studied due to the requirements for integration, stability, and reliability [6, 7]. However, analog PLLs consisting of a phase comparator, filter, and voltage-controlled oscillator (VCO) have problems in terms of generating quick clock signals because of the long time required to reach a steady state after an input signal is applied. Multiplication-type DPLLs have also been proposed, but all proposals have complex circuit configurations. Also, PLLs with an all-digital configuration using a time-to-digital converter (TDC) have also been widely studied. However, the circuit scale is large because it requires a digitally controlled oscillator (DCO) that includes a varactor array of capacitors, an integrating circuit, and an accumulator, and several periods of the input signal are required to generate the clock signal.

On the other hand, a frequency multiplier can generate various frequencies with a simpler circuit configuration and control method than a PLL. However, in a frequency multiplier with an analog configuration, it was difficult to generate an output signal with a frequency that is precisely multiplied with respect to the input signal. This circuit had the problem of requiring resistors, capacitors, etc., even in integration. Also, a frequency multiplier circuit with digital control has been proposed [8, 9], but the conventional circuit uses a counter that counts only the rising edge of the reference clock. For this reason, in the circuit in [8], the input signal and the reference clock were not locked, and the count error occurred in less than one cycle of the reference clock. As a result, the steady-state frequency error of the output signal occurred for a time width of one cycle of the reference clock at most. Therefore, this circuit required a reference clock with a frequency high enough relative to the frequency of the input signal to be practical. In addition, the circuit in [9] has the drawback that the output signal is concentrated in the first cycle of the input signal, so its pulse width is not even.

In this paper, we propose the digital frequency multiplier based on the double-edge counter [10, 11]. The proposed frequency multiplier uses the double-edge counter that counts both the rising and falling edges of the reference clock as the control counter in the circuit. By using this counter, the counting error can be less than half the period of the reference clock. Therefore, the steady-state frequency error of the output signal with respect to the frequency of the input signal can be reduced to one half of that of the conventional circuit. Also, after the input signal is applied, a multiplied output signal can be obtained from one cycle later. Furthermore, since the proposed frequency multiplier is an all-digital configuration, it is easy to integrate and can be expected to be used as a clock supply circuit in various systems.

In the following sections, Chapter 2 describes the circuit configuration and basic operation of the double-edge counter that forms the basis of the proposed circuit, and Chapter 3 describes the circuit configuration of the proposed frequency multiplier based on the double-edge counter and its operation analysis. Chapter 4 presents the simulation results using Verilog-HDL. Finally, Chapter 5 presents conclusion.

2. Double-Edge Counter as Basis of the Proposed Frequency Multiplier.

2.1. Circuit configuration of double-edge counter.

Figure 1 shows the circuit configuration of the double-edge counter that forms the basis of the proposed frequency multiplier. Here, reg1 and reg2 are registers that store values from the "+1" circuit on the rising and falling edges of the reference clock, respectively. The selector selects the value of reg1 when the reference clock is "1" and the value of reg2 when the reference

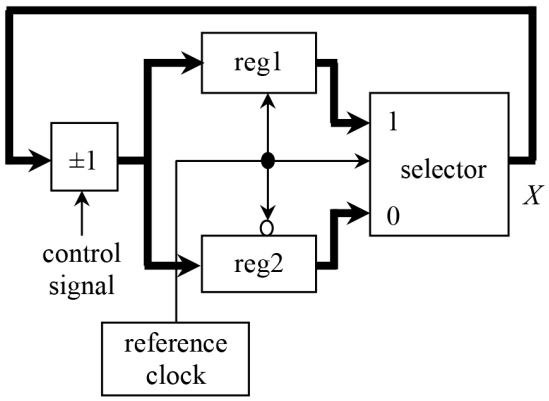

FIGURE 1. Circuit configuration of double-edge counter

clock is "0". The "+1" circuit is an adder that adds "1" to the output value from the selector to supply values to the two registers.

2.2. **Basic operation of double-edge counter.** Figure 2 shows the operating waveform of the double-edge counter. If the value of reg2 before t_0 is "X", the reference clock is "0" and the selector outputs the value "X" of reg2. When the reference clock rises at time t_0, reg1 stores the value "$X + 1$", which is added by "1" to the value "X" from the selector by the "+1" circuit. Then, since the reference clock is "1", the selector selects the value "$X + 1$" of reg1. When the reference clock falls at time t_1, reg2 stores the value "$X + 2$", which is added by "1" to the value "$X + 1$" from the selector by the "+1" circuit. After that, the reference clock is "0", so the selector again selects the value "$X + 2$" for reg2. Thereafter, since the double-edge counter repeats the same operation, the selector outputs the value counted every half period of the reference clock.

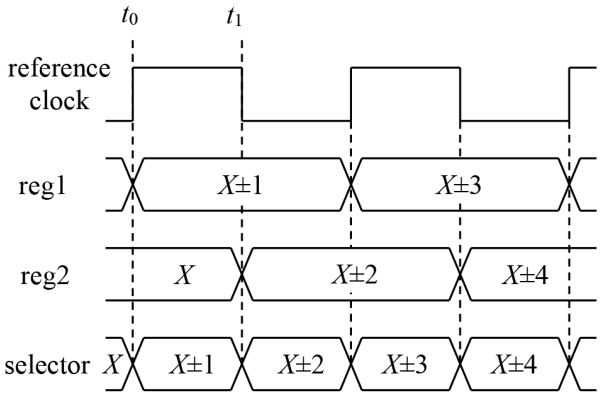

FIGURE 2. Operating waveforms of double-edge counter

3. Proposed Frequency Multiplier Based on Double-Edge Counter.

3.1. **Circuit configuration of the proposed frequency multiplier.** Figure 3 shows the circuit configuration of the proposed frequency multiplier based on the double-edge counter. This circuit consists of two double-edge counters (D-counter1, D-counter2), two counters (counter1, counter2), a 1/2 divider (1/2), two latch circuits (latch1, latch2), and four digital comparators (DC1-DC4).

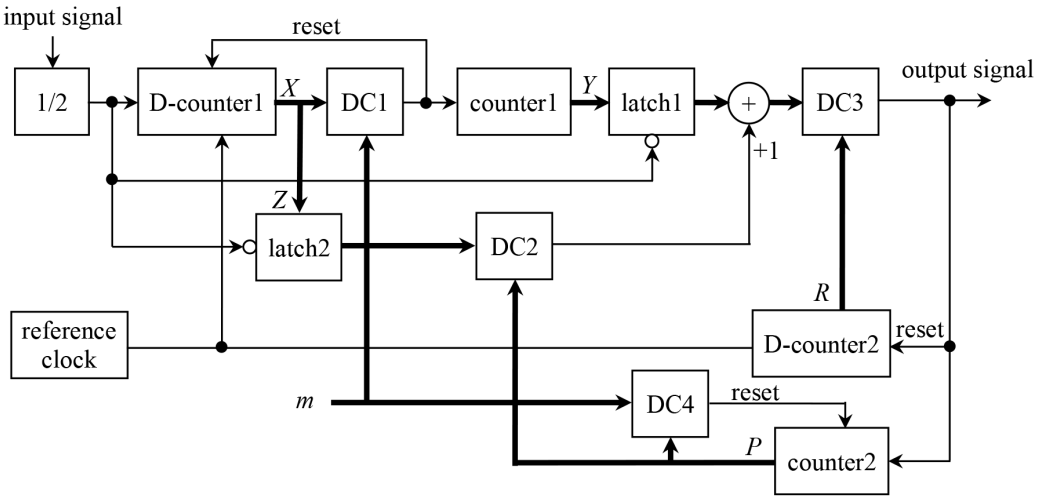

FIGURE 3. Circuit configuration of the proposed frequency multiplier

The counter1 and counter2 are normal counters that perform counting operations at the rising edge of the clock. D-counter1 and counter1 are counters that count the values that determine the multiplication operation, respectively. D-counter2 and counter2 are counters that count the reference clock and output signal to generate the output signal, respectively. The 1/2 divider divides the input signal using its rising edge, and D-counter1 operates only when its output is "1". The latch1 and latch2 store the values of counter1 and D-counter1, respectively, by the falling edge of the output signal of the 1/2 frequency divider. The DC1 compares the multiplication ratio "m" and the value of D-counter1, and when they match, it counts up counter1 and resets D-counter1 at the same time. The DC2 compares the values of latch2 and counter2 and adds "+1" to the value of latch1 according to the result. The DC3 compares the values of D-counter2 and latch1 and outputs a multiplied output signal. The DC4 compares the the multiplication ratio "m" and the value of counter2, and resets counter2 when they match. X, Y, R, and P are the count values of D-counter1, counter1, D-counter2, and counter2, respectively. Also, Z is the remainder value after the counting operation of D-counter1 is completed.

3.2. **Basic operation of the proposed frequency multiplier.** Figure 4 shows the operating waveforms of the proposed frequency multiplier based on the double-edge counter. When the input signal is applied at time t_0, the output of the 1/2 divider is "1". The D-counter1 counts the number of both rising and falling edges of the reference clock that pass during this period. In other words, it counts the number of both edges of the reference clock that pass during one cycle of the input signal. The counter1 counts up by "1"

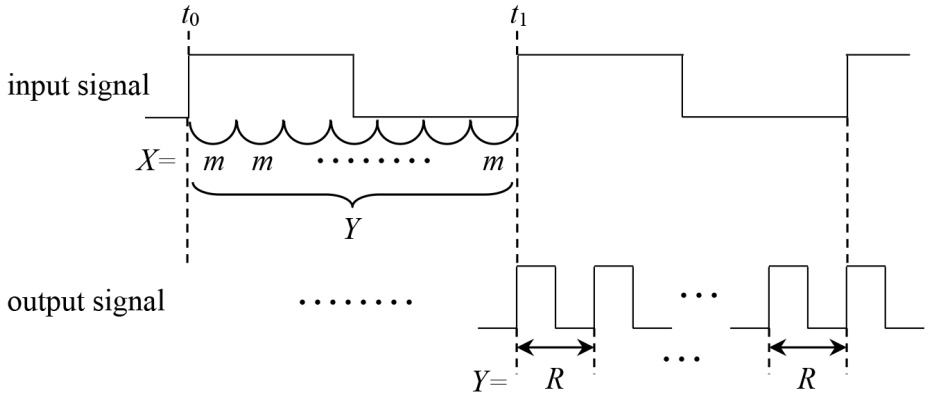

FIGURE 4. Operating waveforms of the proposed frequency multiplier

when the count value "X" of D-counter1 reaches the multiplication ratio "m". The count value of D-counter1 is reset by DC1 at that point and the next counting operation begins. From this operation, the value "Y" of counter1 is the result of dividing the number of both edges of the reference clock that pass during one cycle of the input signal by the multiplication ratio "m". Next, when the output of the 1/2 divider becomes "0" at time t_1, latch1 stores the value "Y" of counter1. The DC3 compares this "Y" with the value "R" of D-counter2, which counts the reference clock, and outputs a multiplied output signal when "$R = Y$". At the same time, D-counter2 is reset. Thereafter, by repeating the same operation, the proposed frequency multiplier can obtain an output signal that is m-multiplied from the input signal.

From the above operation, immediately after the input signal is applied to the proposed frequency multiplier, it is possible to generate a multiplying output signal in one cycle of the input signal. Also, D-counter1 and counter1 perform a counting operation once every two cycles of input signal, and the number of reference clocks required for the multiplication operation is calculated. Therefore, even when the frequency of the input signal changes, the output signal can be generated within two periods of input signal.

3.3. **Dispersion control of the remainder count value.** As described in Section 3.2, the proposed frequency multiplier is controlled by dividing the number of both edges of the reference clock that pass through during one cycle of the input signal by the multiplication ratio "m". However, as shown in Figure 5, if there is a remainder "Z" in the result of the division, that value will be generated as a frequency error in the output signal. Therefore, to obtain a more accurate frequency of the multiplied output signal with respect to the input signal, the remainder "Z" must be included in the output signal generation operation. However, if this "Z" is inserted into any period of the output signal, only the time width of that period becomes wider, and this is a factor that increases the jitter of the output signal in the steady state. For this reason, in the proposed frequency multiplier, the remainder "Z" is controlled so that it is distributed in each period of the output signal.

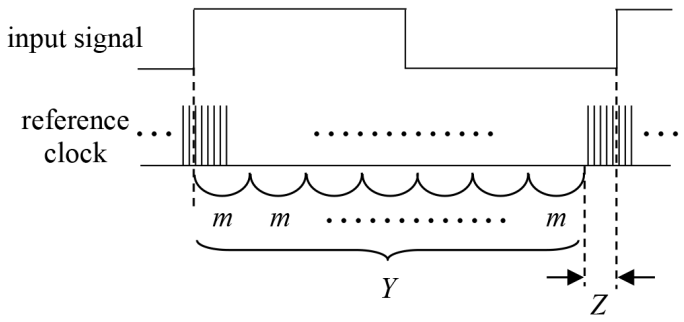

FIGURE 5. Occurrence of remainder Z

Next, we discuss the dispersion control of the remainder value. Figure 6 shows the operating waveforms in the dispersion of the remainder values. The remainder "Z" is the value of D-counter1 at the time when the 1/2 divider value becomes "0". The latch2 stores the value of D-counter1 corresponding to the remainder "Z" at this point. The DC2 compares "Z" with the value "P" of counter2, which counts the number of output signal clocks. While the relationship between the compared values is "$Z \geq P$", the remainder "Z" is distributed to each period of the output signal by adding "1" to the value "Y" of latch1 as shown in Figure 6(b). Also, the counter2 is reset by DC4 when its count reaches the multiplication ratio "m". By repeating the above operation, the proposed multiplier circuit removes the frequency error of the output signal related to the remainder "Z".

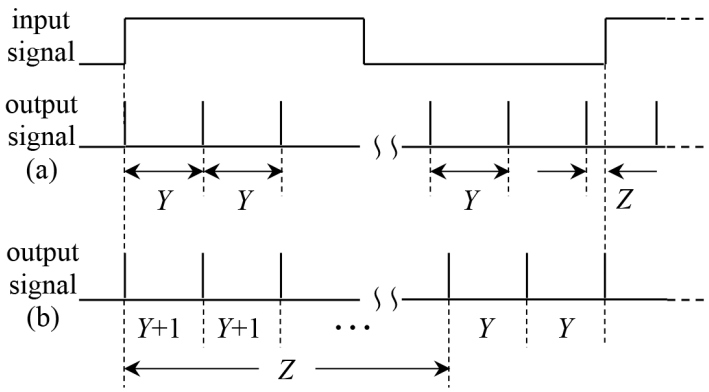

FIGURE 6. Operating waveforms of remainder control

3.4. **Operation analysis.** Next, we consider the output jitter of the proposed frequency multiplier. This circuit removes frequency errors in the output signal by dispersion controlling of the remainder value as described in Section 3.3. However, this dispersion process does not add equally to all cycles of the output signal. Here, if the time for one output signal cycle is T_{out}, the time for one input signal cycle is T_{in} and the time for one half cycle of the reference clock is t_{clk}, the relationship is expressed as follows:

$$T_{out} = \begin{cases} \left\lfloor \dfrac{T_{in}}{m \cdot t_{clk}} \right\rfloor \cdot t_{clk} \\ \left\lfloor \dfrac{T_{in}}{m \cdot t_{clk}} \right\rfloor \cdot t_{clk} + t_{clk} \end{cases} \tag{1}$$

From this equation, if the counting operation for one cycle of the input signal produces a remainder, the output signal will have an output jitter of half the period of the reference clock. Therefore, if the frequencies of the input signal and the reference clock are f_{in} and f_{clk}, respectively, the ratio σ_{err} of the output jitter to the input signal is

$$\sigma_{err} \leq \frac{m \cdot f_{in}}{2 f_{clk}} (\%) \tag{2}$$

From the above, when the proposed frequency multiplier is used as a clock source for various systems, etc., each value should be set according to the allowable output jitter.

In addition, the input signal of the proposed frequency multiplier and the reference clock are not locked. Hence, this circuit will have timing errors of less than half a cycle of the reference clock at the beginning and end of counting the number of both edges of the reference clock that pass during one cycle of the input signal at D-counter1, respectively. Although these timing errors will cancel each other out, errors of less than half a period of the reference clock will eventually occur. This error shows up as a frequency error in the output signal. Therefore, the setting of each value should take this timing error into account when designing.

4. **Simulation Results.** The operation of the proposed frequency multiplier was verified by simulation using Verilog-HDL, a hardware description language.

Figure 7 shows the simulation results from the time an input signal is applied to the proposed frequency multiplier until the output signal is generated. In the simulation, as an example of operation verification, the multiplication ratio is set to "$m = 4$", the frequency of the input signal to 20 kHz, and the frequency of the reference clock to 240 kHz, respectively. The input signal is applied at time t_0. Subsequently, at time t_1, "$Y = 12$", which determines the frequency of the output signal, and "$Z = 1$", the remainder values when calculating Y, are determined, respectively. From this, it is found

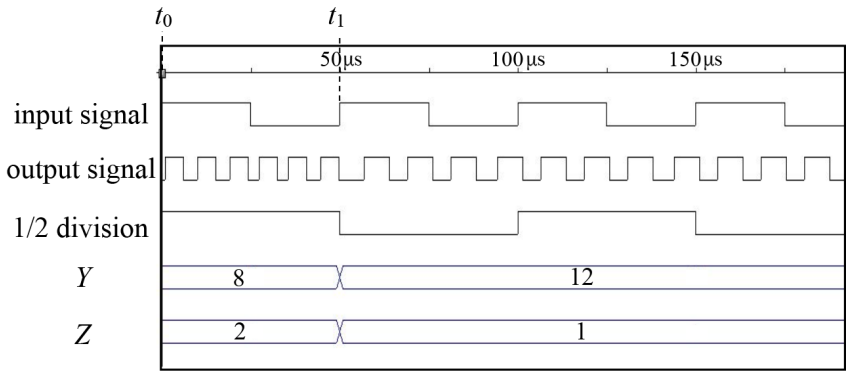

FIGURE 7. Simulation results after adding input signal

that the proposed frequency multiplier is able to achieve multiplication operation in a single cycle period after the input signal is applied.

Figure 8 shows the simulation results when the frequency of the input signal changes during multiplication operation. The multiplication ratio and the frequency of the reference clock are set to "$m = 4$" and 240 kHz, respectively. At time t_0, the frequency of the input signal changes from 20 kHz to 35 kHz. Subsequently, at time t_1, "$Y = 7$", which determines the frequency of the multiplied output signal, and "$Z = 2$", the remainder values when calculating Y, are determined, respectively. From this, it is found that when the frequency of the input signal changes, the output signal can be generated within two cycles. It can also be seen that the remainder value "$Z = 2$" is distributed in each period of the multiplied output signal.

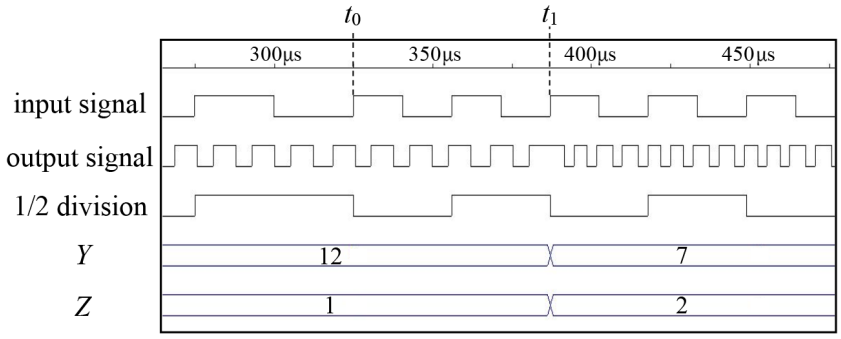

FIGURE 8. Simulation results when input signal changes

Figure 9 shows the simulation results when the multiplication ratio is changed during the multiplication operation. The frequencies of the input signal and the reference clock are set to 20 kHz and 240 kHz, respectively. At time t_0, the multiplication ratio "m" changes from "4" to "7". Subsequently, at time t_1, "$Y = 6$", which determines the frequency of the multiplied output signal, and "$Z = 6$", the remainder values when calculating Y, are determined, respectively. From this, it is found that even when the multiplication ratio is varied, the output signal can be generated within two periods of the input signal.

5. **Conclusion.** In this paper, we proposed the frequency multiplier based on the double-edge counter. This circuit uses the double-edge counter that counts both edges of the reference clock and corrects the remainder when counting, so that the steady-state frequency error of the output signal relative to the frequency of the input signal can be less than half the period of the reference clock. As a result, the steady-state frequency error can be

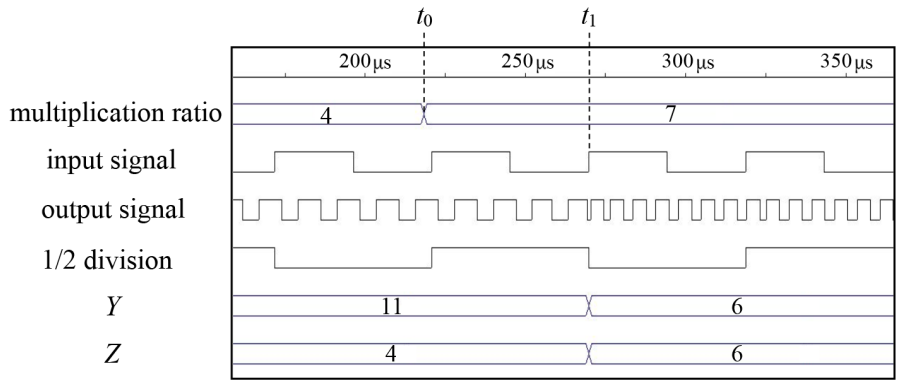

FIGURE 9. Simulation results when the multiplying ratio is changed

reduced to 1/2 that of the conventional method. Also, the output signal can be generated one cycle after the input signal is applied. Furthermore, if the frequency of the input signal or multiplication ratio changes during multiplication operation, the desired output signal can be obtained within two periods of the input signal. In the future, we intend to reduce the steady-state frequency error by using a multi-phase clock in the frequency multiplier.

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REFERENCES

[1] D. Nishiguchi, M. Fukuhara, M. Yahara and K. Fujimoto, Hamming distance search circuit using interconnect capacitance, *ICIC Express Letters*, vol.17, no.6, pp.659-665, 2023.

[2] Y. Harada, M. Yahara, K. Eguchi and K. Fujimoto, Flash type A/D converter using neuron CMOS inverters with threshold compensation circuits, *ICIC Express Letters*, vol.14, no.3, pp.251-256, 2020.

[3] M. Miyazaki and K. Ishibashi, A 3-cycle lock time delay-locked loop with a parallel detector as a low-power system-clock generator, *IEICE Transactions on Electronics*, vol.J83-C, no.6, pp.502-508, 2000.

[4] K. Eguchi, A. Shibata, T. Ishibashi and I. Oota, An inductor-less nesting-type step-up/step-down ac/ac converter with a small component count, *International Journal of Innovative Computing, Information and Control*, vol.15, no.6, pp.2377-2384, 2019.

[5] Y. Harada, M. Yahara, K. Matsumoto and K. Fujimoto, A programmable divider with 50% duty cycle unrelated to dividing cycle and its application to PLL, *IEEJ Transactions on Electronics, Information and Systems*, vol.136, no.1, pp.2-7, 2016.

[6] M. Yahara, K. Fujimoto and H. Kiyota, Multiple frequency digital phase-locked loop based on multi-phase clock divider with constant pulse interval, *IEEJ Transactions on Electronics, Information and Systems*, vol.138, no.4, pp.387-394, 2018.

[7] M. Yahara, K. Fujimoto and D. Nishiguchi, A study of digitally controlled oscillator based on multi-phase clock, *IEEJ Transactions on Electronics, Information and Systems*, vol.141, no.7, pp.840-841, 2021.

[8] N. Boutin and A. Boucher, A novel digital frequency multiplier, *IEEE Transactions on Instrumentation and Measurement*, vol.IM-35, no.4, pp.566-570, 1986.

[9] H. Sasaki, H. Yahara, K. Fujimoto and F. Ueno, A m-times pulse number generating circuit based on SC bootstrap type monostable multivibrator and its application, *IEICE Transactions on Electronics*, vol.J78-C2, no.6, pp.331-338, 1995.

[10] K. Fujimoto, H. Sasaki and M. Yahara, A dividing ratio changeable digital PLL based on phase state memory and double-edge detection, *IEEJ Transactions on Electronics, Information and Systems*, vol.128, no.7, pp.1185-1190, 2008.

[11] M. Yahara, K. Fujimoto, D. Nishiguchi and Y. Harada, Digital frequency-locked loop based on double-edge counter, *ICIC Express Letters, Part B: Applications*, vol.12, no.5, pp.427-434, 2021.