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ANALOG CMOS IMPLEMENTATION OF ISING-BASED TRAFFIC LIGHTS CONTROL UNIT

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Abstract. *In conventional studies on traffic light control (TLC), the theory of Ising-based TLC system was proposed. The Ising-based TLC system is used to alleviate traffic congestion in urban cities with heavy traffic. However, hardware implementation of the Ising-based TLC system has not been studied. In this paper, we propose an Ising-based TLC unit on hardware of transistor level. The circuit of the proposed TLC unit is designed according to Rohm 0.18μm CMOS rule, and its operation is verified by HSPICE simulation.*

Keywords: Traffic light control, Ising-model, CMOS circuit, Self-organization, Urban road network, Hybrid dynamical system

1. **Introduction.** Traffic congestion causes big economic losses in urban cities with heavy traffic. In the United States, traffic congestion causes economic losses of over $100 billion annually [1]. In the European Union, the cost of traffic congestion is estimated at 1% of GDP [2]. The cause of traffic congestion in urban cities is increasing disparities between highway capacity and vehicular population [3]. Therefore, traffic light controller (TLC) is being researched as a strategy to solve traffic congestion [4-10]. These studies aim to control traffic flow by giving traffic lights intelligent rules. Intelligent rules include rules that use self-organization [4,5], use AI [6,7], and use fuzzy logic [8]. The TLC studies are comprehensively described in [10]. The TLC systems are implemented with microcontrollers, FPGAs, ASICs, and more [9]. Recently, the theory of Ising-based TLC system was proposed as one of the new TLC systems [12]. In this theory, Ising-based TLC units are placed at each intersection to optimize traffic flow while interacting with adjacent intersections. Because the Ising-based TLC is self-organizing, it has the potential to make a significant contribution to solve traffic congestion. However, hardware implementation of the Ising-based TLC system has not been studied. In this paper, we propose an Ising-based TLC unit hardware on transistor level. The proposed hardware is designed according to Rohm 0.18μm CMOS rule, and its operation is verified by HSPICE simulation. In the next section, we describe the theory of Ising-based TLC system. A block diagram of the Ising-based TLC hardware is shown, a transistor-level schematic of each block is clarified, and their operation is explained in Section 3. The simulation result of the Ising-based TLC unit circuit designed according to the Rohm 0.18μm rule is shown, and the problem is considered from the waveform in Section 4. Section 5 summarizes this paper and gives directions for our future study.

2. **The Theory of Ising-Based TLC System.** The theory of Ising-based TLC system was proposed [12]. According to the theory of Ising-based TLC system, Ising-based TLC units are located at all node $N(i)$ of a two-dimensional grid network as shown in Figure 1(a). The $N(i)$ denotes an intersection as shown in Figure 1(b), and four intersections

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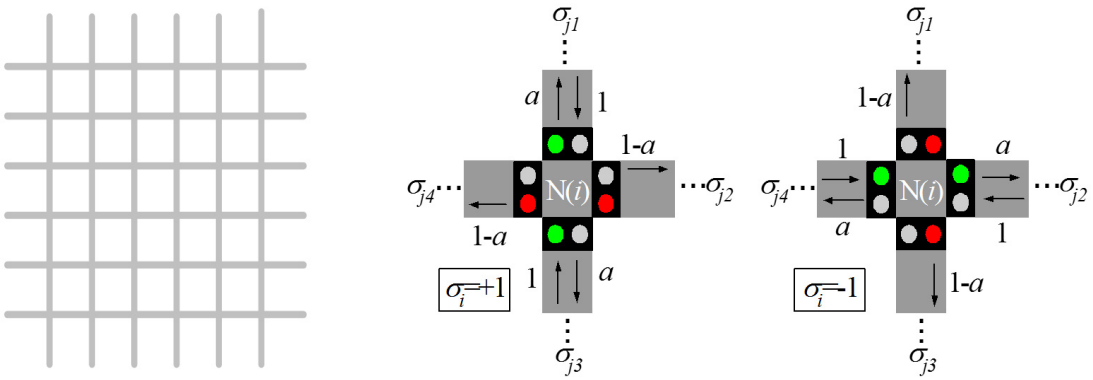


(a) (b)

FIGURE 1. Ising-based TLC system: (a) Two-dimensional grid network and (b) Ising-based TLC unit

$N(j)$ are adjacent to $N(i)$. There are two lanes between the intersections $N(i)$ and $N(j)$. Vehicles are considered as fluids flowing along the lane; they flow into $N(i)$ and flow out into the adjacent $N(j)$. The traffic light located at $N(i)$ has two states, $\sigma_i = \{-1, +1\}$. When $\sigma_i = +1$, vehicles in the vertical lane are allowed to flow into $N(i)$, and when $\sigma_i = -1$, vehicles in the horizontal lane are allowed to flow into $N(i)$. Vehicles flow into $N(i)$ at a rate of 1 unit time. After, vehicles go straight by the amount of a, and turns right or left by the amount of $1 - a$, where $a \in [0, 1]$ is a parameter of the model. The dynamics of the traffic light change according to the differential Equation (1).

$$\frac{dx_i}{dt} = -\sigma_i + \frac{\alpha}{4} \sum_{j \in N(i)} \sigma_j \tag{1}$$

where α denotes $2a - 1$ and $N(i)$ denotes a set of four intersections adjacent to the i-th intersection. When $\sigma_i = +1$, x_i does not increase and when $\sigma_i = -1$, it does not decrease, because $-1 \leq \alpha \leq +1$. In addition, σ_i is changed to $+1$ when x_i reaches $+\theta$, and σ_i is changed to -1 when x_i reaches $-\theta$, as in Equation (2).

$$\begin{aligned} \sigma_i &\leftarrow +1 \text{ when } x_i \geq +\theta \\ \sigma_i &\leftarrow -1 \text{ when } x_i \leq -\theta \end{aligned} \tag{2}$$

The above is the theory of Ising-based TLC system. Since the Ising-based TLC unit has not been implemented yet, we design the Ising-based TLC unit hardware using an analog CMOS circuit. Figure 2 shows the behavior of Ising-based TLC unit when parameter a is set to 1/4. Figure 2(a) shows behavior of TLC unit when the number of $+1$ in σ_j is two, Figure 2(b) shows when σ_j is all $+1$ and Figure 2(c) shows TLC when σ_j is all -1. These cases are used as performance evaluation indexes for the Ising-based TLC unit circuit.

3. Design of Ising-Based TLC Unit.

The proposed circuit consists of a σ_i circuit, a σ_j circuit, a current control (CC) circuit, and a pulse control (PC) circuit, as shown in Figure 3.

3.1. The Gilbert multiplier.

Figure 4 shows the Gilbert multiplier. The σ_i circuit and σ_j circuit are composed of Gilbert multipliers. The Gilbert multiplier outputs the current I_{out} based on Equation (3).

$$I_{out} = I_b \tanh \frac{k\left(V_\sigma - \bar{V}_\sigma\right)}{2} \tanh \frac{k\left(V_p - V_n\right)}{2} \tag{3}$$

V_σ represents σ composed of binary values of "+1", "−1" by applying V_{DD} or 0[V]. Reverse the sign of the current I_{out} according to the magnitude relationship between V_p and V_n.

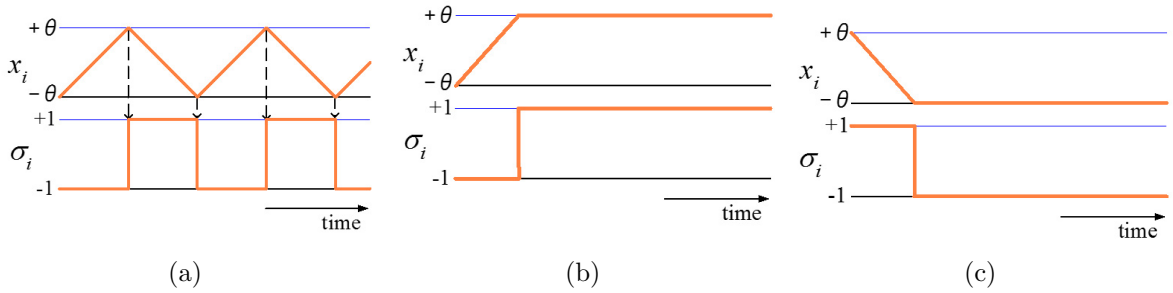


FIGURE 2. Behavior of Ising-based TLC unit: (a) Case with duty ratio of 0.5; (b) the case where σ_i is $+1$ and the system stops; (c) the case where σ_i is -1 and the system stops

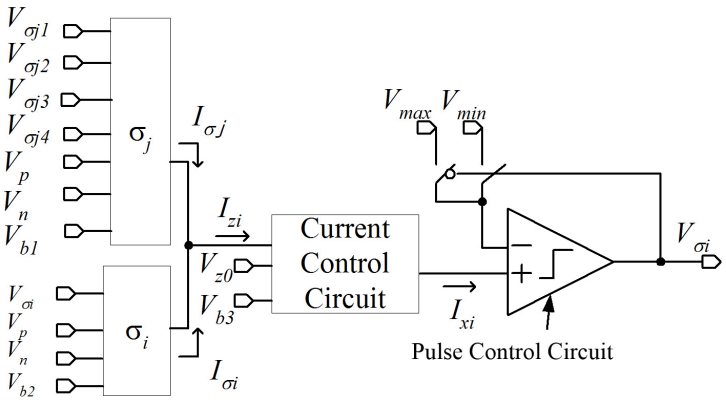


FIGURE 3. The block diagram of Ising-based TLC unit

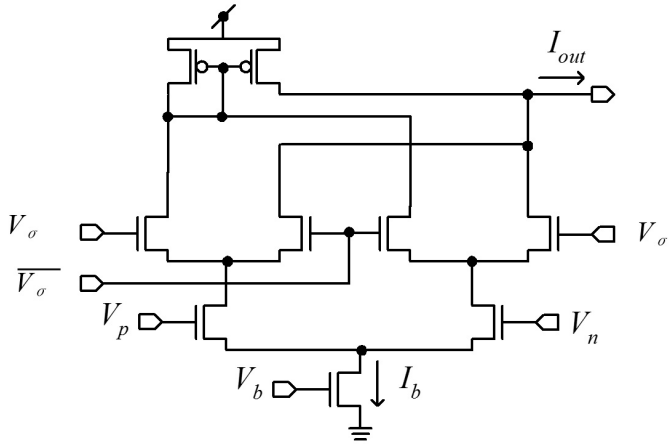
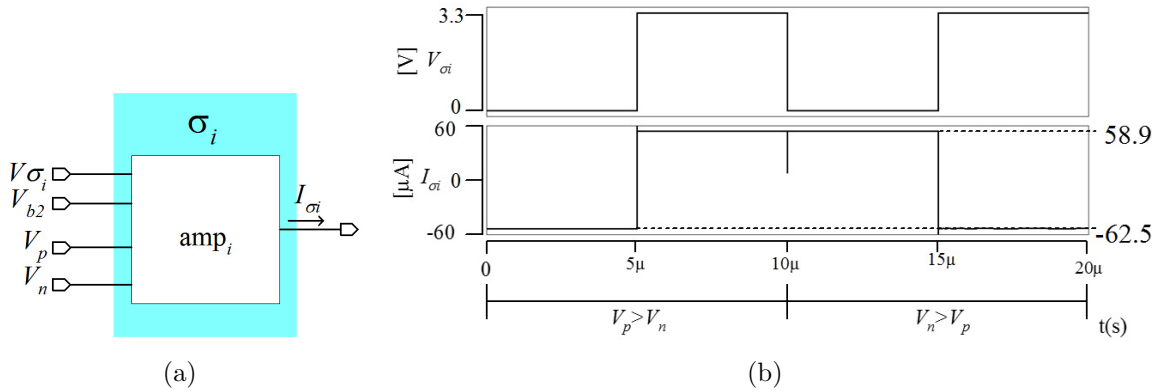


FIGURE 4. The Gilbert multiplier

And manipulating V_b between 0[V] and V_{DD}, $\alpha/4$ represented by $-1/4$ to $1/4$ is expressed. This circuit block is named "amp".

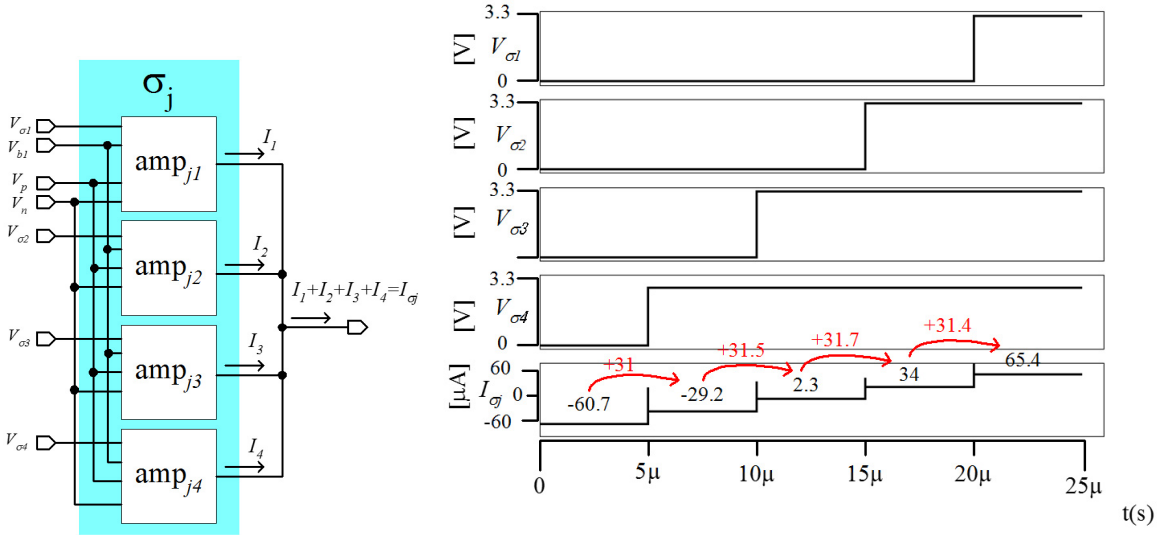
3.2. **Operation of σ_i circuit.** Figure 5 shows the block diagram and operation of the σ_i circuit. The σ_i circuit is a circuit block for realizing $-\sigma_i$ in Equation (1) and is composed of one Gilbert multiplier (amp). The σ_i circuit is designed to obtain $+1$ output current when V_{DD} is applied to $V_{\sigma i}$ and -1 output current when 0[V] is applied. Also, set $V_p < V_n$, invert the sign and set V_{b2} to V_{DD}.

3.3. **Operation of σ_j circuit.** Figure 6 shows the block diagram and operation of the σ_j circuit. The σ_j circuit is a circuit for realizing $\frac{\alpha}{4}\sum_{j\in N(i)}\sigma_j$ in Equation (1) and is realized



(a) (b)

FIGURE 5. Operation of σ_i circuit: (a) Block diagram of σ_i circuit and (b) operation of σ_i circuit



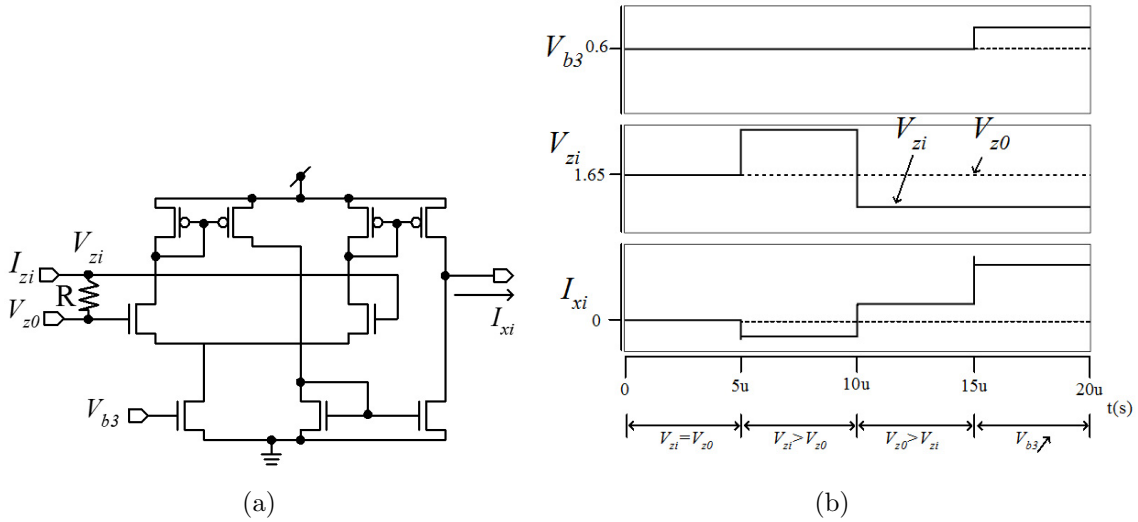
(a) (b)

FIGURE 6. σ_j circuit: (a) Block diagram of σ_j circuit and (b) operation of σ_j circuit

by wiring addition the output currents of four amps. In this paper, V_{b1}, V_p, and V_n are common parameters for all multipliers. The $V_{\sigma 1}$-$V_{\sigma 4}$ is designed to obtain $+1$ output current when V_{DD} is applied to $V_{\sigma 1}$-$V_{\sigma 4}$ and -1 output current when 0[V] is applied. Figure 6(b) shows the operation of the σ_j circuit when $V_p > V_n$ and V_{b2} are set to 0.7[V].

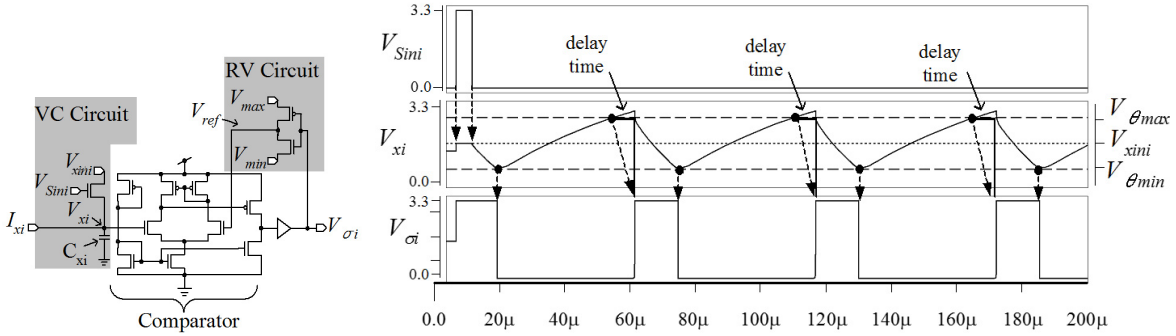
3.4. **Operation of current control circuit.** Figure 7 shows the schematic and operation of the CC circuit. The CC circuit is a circuit for limiting the amount of current flow to the PC circuit. R is a resistor that converts the current I_{zi} into a voltage. When $V_{zi} = V_{z0}$, the output is 0[A], when $V_{zi} > V_{z0}$, a negative current flow, when $V_{zi} < V_{z0}$, a positive current flow, and the amount of current can be changed with V_{b3}.

3.5. **Operation of pulse control circuit.** Figure 8 shows the schematic and operation of the PC circuit. The PC circuit realizes Equation (2). The PC circuit consists of a voltage calibration (VC) circuit, a reference voltage (RV) circuit, and a comparator. In the VC circuit, V_{xi} is set to V_{xini} when V_{Sini} rises. In the RV circuit, $V_{\max}$ is set to V_{ref} when $V_{\sigma i}$ is 0[V], and V_{ref} is set to $V_{\min}$ when $V_{\sigma i}$ is V_{DD}. In the comparator, V_{xi} and V_{ref} are compared, and $V_{\sigma i}$ is changed according to Equation (2).



(a) (b)

FIGURE 7. CC circuit: (a) Schematic of CC circuit and (b) operation of CC circuit



(a) (b)

FIGURE 8. PC circuit: (a) Schematic of PC circuit and (b) operation of PC circuit

4. **HSPICE Simulation Result.** We designed the Ising-based TLC unit circuit with the model parameters shown in Table 1(a) according to the Rohm 0.18μm rule and verified HSPICE simulation under the input voltage conditions shown in Table 1(b). Figure 9 shows HSPICE simulation results of the Ising-based TLC unit circuit. Depending on the input voltage conditions of V_{b1}, V_p, and V_n, $\alpha/4$ is considered to 1/4. Therefore, from Equation (1), when $\sum_{\sigma j} = -4$, the $V_{\sigma i}$ is constant of 0[V], when $\sum_{\sigma j} = +4$, the $V_{\sigma i}$ is

TABLE 1. Simulation parameter: (a) Rohm 0.18μm process rule and (b) input voltage conditions

(a)

Symbol	Value	Units
V_{DD}	3.3	V
GND	0	V
C	16	fF
R	6.9	kΩ
W_n/L_n	1.0/0.36	μm
W_p/L_p	3.0/0.30	μm

(b)

Pin name	Value	Units
V_p	1	V
V_n	0	V
V_{b1}	0.7	V
V_{b2}	3.3	V
V_{b3}	0.6	V
$V_{\max}$	1.5	V
$V_{\min}$	1	V
V_{xini}	1.3	V
V_{z0}	1.65	V

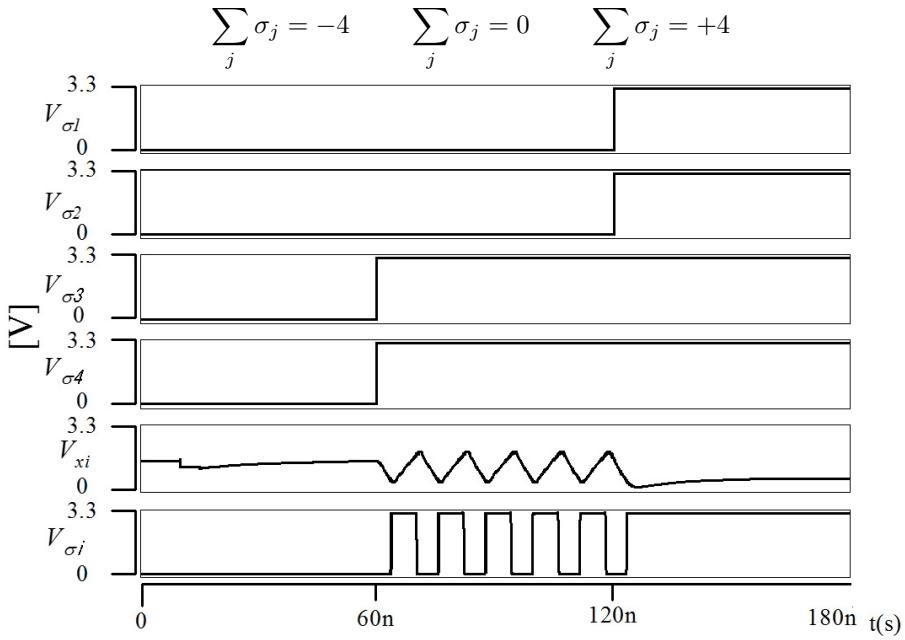


FIGURE 9. Ising-based TLC unit circuit HSPICE simulation result

constant of V_{DD}, when $\sum_{\sigma j} = 0$, the duty ratio of the output voltage $V_{\sigma i}$ is 0.5. In the HSPICE simulation result shown in Figure 9, the duty ratio of $V_{\sigma i}$ when $\sum_{\sigma j} = 0$ is 0.45, the results were almost as theoretical.

5. **Conclusions.** In this paper, we proposed a hardware design method using a CMOS circuit for the Ising-based TLC unit. The operation of the proposed circuit was verified by HSPICE simulation, and it was confirmed that the proposed circuit operates according to theory, although the characteristics deviated. In the future research, we will optimize the proposed circuit and aim to implement the Ising-based TLC system.

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