ICIC Express Letters
Part B: Applications
Volume **13**, Number **6**, June **2022**

ICIC International ©2022 ISSN 2185-2766
pp. 553–561

A 4 V, 100 MA LOW DROPOUT VOLTAGE REGULATOR (LDO) FOR MOBILE PHONE SOLAR CHARGER APPLICATION

Antonius Irianto Sukowati[1], Eri Prasetyo Wibowo[2,*], Dyah Nur'ainingsih[3] and Robby Kurniawan Harahap[2]

[1]Electronic Engineering Department
Cendekia Abditama University
Jl. Islamic Raya No. 1 Tangerang, Banten 15810, Indonesia
irianto@cendekia.ac.id

[2]Center for Microelectronics and Image Processing Studies
[3]Electronic Engineering Department
Gunadarma University
Jl. Margonda Raya No. 100, Pondok Cina, Depok, Jawa Barat 16424, Indonesia
{ dyahnur; robbyku }@staff.gunadarma.ac.id
*Corresponding author: eri@staff.gunadarma.ac.id

Received July 2021; accepted October 2021

Abstract. *Currently, the battery charging process on mobile phones generally relies on a fixed electricity source or portable power bank which is still relatively big. An independent solar charger system for mobile phone's battery is developed using 0.35 μm CMOS technology. In this system, a low dropout voltage regulator (LDO) is used to stabilize the charging voltage. A CMOS low dropout voltage regulator (LDO) voltage regulator design flow using 0.35 μm CMOS technology is described and simulated in this paper. The LDO consists of PMOS pass transistor, resistive feedback network and simple operational transconductance amplifier (OTA) as the error amplifier. This LDO was designed to mantain stable voltage at 4 V and 100 mA of current output in low resistive load. The experimental result through simulation showed that the LDO has the ability to maintain a regulated output voltage at 4 V from input voltage greater than 4.1 V and maximum output load current is 100 mA. This LDO is able to mantain the voltage and current output to remain stable even though the resistive load is reduced to 40 Ω.*
Keywords: Low dropout regulator, LDO, CMOS, OTA, Voltage regulator

1. **Introduction.** The conventional battery charging process on a mobile phone devices shown in Figure 1 is usually very dependent on fixed power source or using a portable power bank which is still relatively large in size. With current chip technology, an independent charging system that utilizes alternative energy can be integrated into a mobile phone.

The solar energy harvesting system for gadget's battery charging processes is one of the alternatives that can be developed to support the use of renewable energy. Solar energy harvesting for microsystem that has been developed in [1-4] also proposed the voltage regulator which is unfortunately only suitable for driving micro unit of current to the load, while battery charging system in mobile phone requires at least 3.7 V and 100 mA to start the charging process [5].

In developed battery charging system shown in Figure 2, the voltage regulator aims to stabilize the output of DC-DC voltage converter which amplifies the voltage converted by micro solar cells. The voltage regulator must have fast load transient response, high power rejection ratio, good load regulation, low inrush current, and enough bandwidth to react when the input and power supply changes occur [6].

DOI: 10.24507/icicelb.13.06.553

(a) (b)

FIGURE 1. Conventional mobile phone charging: (a) Using fixed electricity; (b) using power bank

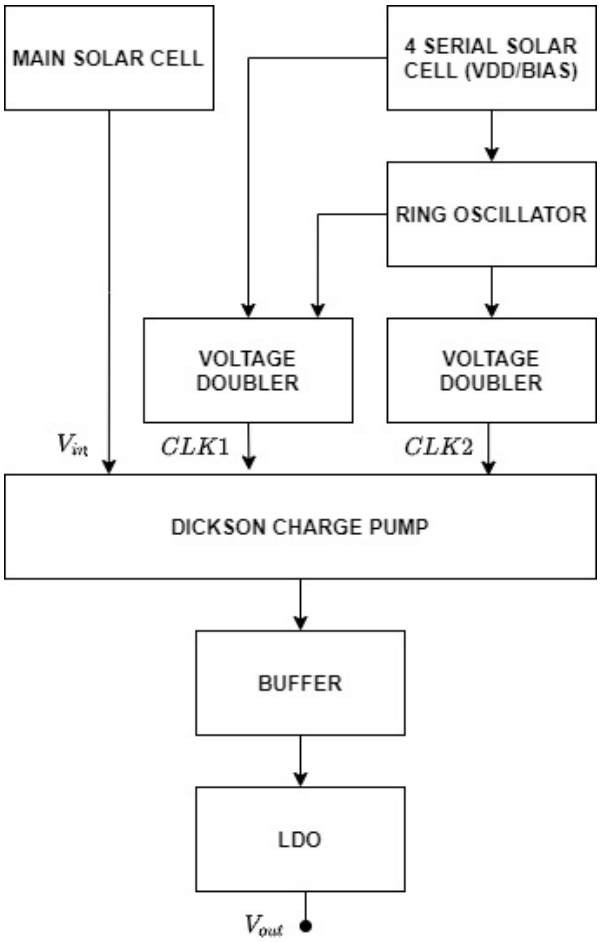


FIGURE 2. Developed solar mobile phone charging system

Low dropout voltage regulator (LDO) has been widely used as a voltage regulator for electronic circuits. It acts as a regulator that stabilizes the output voltage from the fluctuating voltage input. LDO is basically a DC linear voltage regulator with very small input-output differential voltage. Since LDO has characteristics suitable as a voltage regulator and can present a compact size component, it becomes dispensable in a system-on-chip (SoC) power management unit [7, 8]. LDO as part of power management for solar powered systems has been previously studied by [9, 10]. The use of LDO becomes very

important due to the growing need for small portable electronic devices such as mobile phones, tablets, and other gadget devices [11-13].

To meet the requirements mentioned above, several techniques are presented in the design process to realize an LDO with a very simple circuit structure due to limitation of chip area. The LDO was designed under classic topology using operational transconductance amplifier (OTA) as presented by [14-16].

From the simulation, this designed LDO is able to generate the regulated charging voltage and current required to charge the mobile phone's battery with a simple OTA structure to meet a limited area of the chip.

The organization of this paper is as follows: Section 2 describes the proposed LDO design and its specifications, Section 3 discusses the process of the design of the LDO, and Section 4 clarifies the design by explaining the simulation result. At the end of this paper, Section 5 defines the conclusion and the future work of this project.

2. Low Dropout Voltage Regulator Structure and Schematic Design.

The structure of the proposed LDO is presented in Figure 3(a). The LDO consists of several building blocks, i.e., the error amplifier, pass element and feedback resistors. As one of the LDO's building blocks, the error amplifier works as a device that generates error signals for voltage regulation. The output of the error amplifier was then fed into the input of pass element as the next building block. This error amplifier was made of an op-amp arranged by a pair of differential amplifiers and a high output swing common source amplifier in cascade formation. This simple circuit is required to obtain a relatively small area of the LDO chip. Pass element which is made using PMOS transistor functions as the voltage controlled current source. The last part of the LDO was the feedback section that is constructed by using two resistors for connecting the pass element to error amplifier.

The error amplifier was made using an operational transconductance amplifier (OTA) circuit which is composed of NMOS differential pair (M1 and M2) with active load (M3 and M4) in the first stage. The common source stage (M6) in the second stage was biased by a current mirror (M5, M7, and M8). This current was also used to bias the first stage [16-18]. The configuration of this error amplifier is shown in Figure 3(b).

PMOS type of transistor was selected for the pass transistor because it requires only a small input voltage in its gate to work in the saturation region at dropout. An NMOS transistor also can be used as a pass transistor. However, the NMOS transistor requires additional circuitry to increase the gate voltage. As a result, the complexity of the circuit will increase and the chip area will also be affected [19, 20]. The voltage gain of the pass transistor is less than the unity. However, the error amplifier assures that no degradation occurs in the loop gain. The proposed LDO was designed to have 60 dB loop gain and 80 MHz gain bandwidth to achieve good load and line performance as well as its transient response performance.

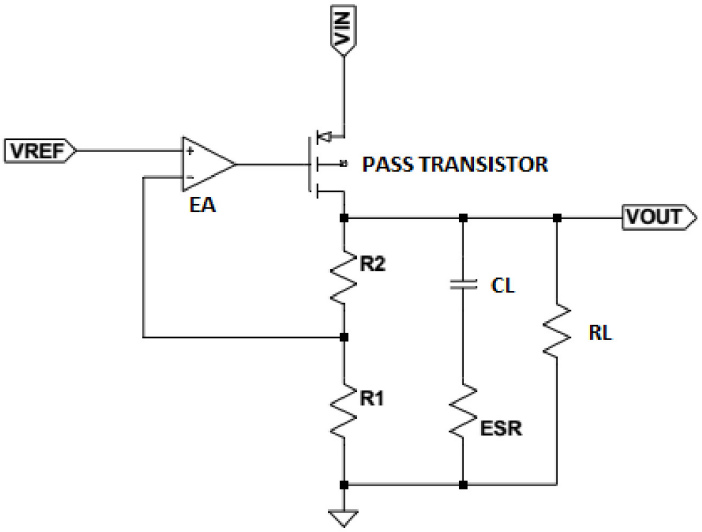
Since the LDO was designed in AMS 0.35 μm CMOS technology, some parameters were used in the entire design (k_n = 189 μA/V^2, k_P = 64 μA/V^2, V_{THN} = 0.46 V and V_{THP} = −0.68 V). These parameters were randomly chosen from the range of standard technology parameters of CMOS AMS 0.35 μm.

3. LDO Voltage Regulator Design.

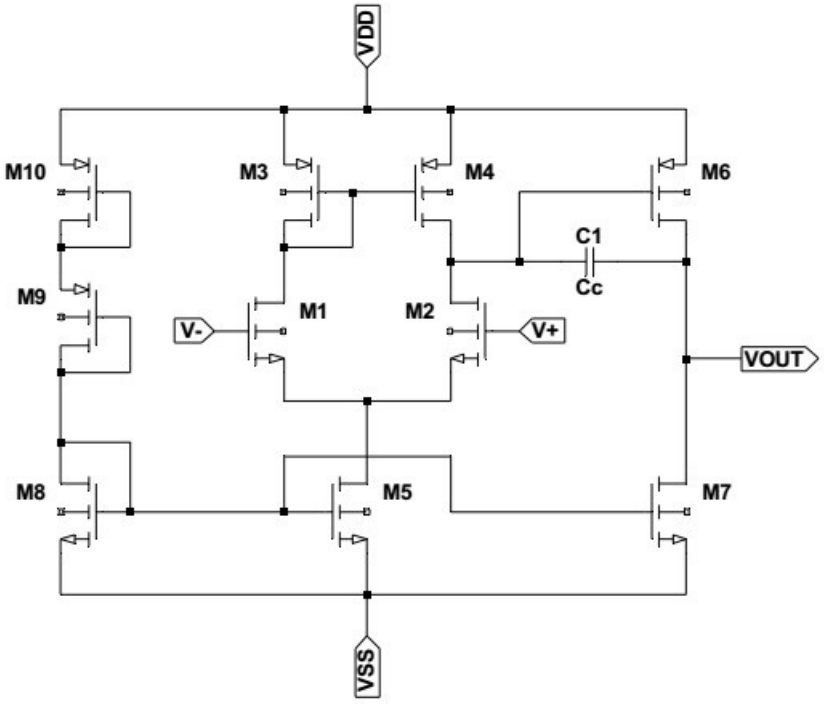
In LDO design processes, there were three steps taken, the first step was to determine the value of the feedback resistors, design of the pass transistor as the second step, then followed by the design of the op-amp used as the error amplifier as the last step.

3.1. Determining the value of feedback resistors.

The voltage reference (V_{REF}) is the voltage that will be compared with the voltage resulting from division divided by resistors R1 and R2. The voltage comparison process was performed in the error amplifier circuit to obtain the voltage which will regulate the work of the pass transistor. V_{REF}



(a)



(b)

FIGURE 3. Topology of system and component: (a) LDO; (b) OTA

can be calculated as the op-amp non-inverting amplifier model using Equation (1). To simplify the calculation process, the same value of R_2 and R_1 was chosen.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \tag{1}$$

3.2. **Pass transistor design.** The second step in the LDO design was to design the pass transistor. The pass transistor was selected from PMOS transistor type in order to achieve low dropout voltage [21]. The calculation of the length and width of the pass transistor channel (W/L) was carried out by considering the drain current (I_{DPASS}), electron mobility (μ_P), oxide capacitance per unit area (C_{ox}), gate-source voltage (V_{GS}), and threshold

voltage (V_{THP}) as in Equation (2). In order to minimize the area, the minimum length of $L_{PASS} = 0.35$ µm was used.

$$\frac{W}{L} = \frac{I_{DPASS}}{\frac{1}{2}\mu_P C_{ox}(V_{GS} - V_{THP})^2} \tag{2}$$

3.3. **Error amplifier design.** The next step in this LDO design was to design an error amplifier that serves as a comparator. The error amplifier was arranged using OTA type of op-amp shown in Figure 3(b) as its core. It was designed to have 80 MHz of gain bandwith (GBW), $\geq$ 60 dB of loop gain, $-45°$ of phase margin (PM), 20 V/µs of slew rate (SR), $\pm$2.673 V of common mode input ratio ($\pm$CMR) and 10 pF of capacitive load.

The design of error amplifier is started by calculating the minimum value of the compensation capacitor (C_C). The load capacitor (C_L) value of 10 pF was included as one of the variables in the calculation according to Equation (3). In practice, a 10 pF load capacitor is useful enough for preventing ripple voltage that might occur when the LDO is connected to the load.

$$C_C = \frac{2.2}{10} C_L \tag{3}$$

As the minimum compensation capacitor set, transconductance for transistors M1 and M2 (gm_1 and gm_2) was then calculated using gain bandwidth (GBW) from OTA design specification. Since both transistors M1 and M2 were in identical type and size, gm_1 and gm_2 also had the same value. The transconductance of M1 and M2 was calculated using Equation (4)

$$gm_{1,2} = GBW \cdot 2\pi \cdot C_C \tag{4}$$

The gm_1 value which was equal to the gm_2 resulted in the same value of drain current (I_D) flowing through M1 and M2, $I_{D1} = I_{D2} = \frac{I_{SS}}{2}$, where I_{SS} is the current flowing on the transistor M5, I_5. The calculation of this current was conducted based on slew rate (SR) and the compensation capacitor (C_C) as shown in Equation (5).

$$I_{D1} = I_{D2} = \frac{SR}{2} C_C \tag{5}$$

Once the transconductance of M1 and M2 set, the dimension of M1 and M2 was then calculated. The size of M1 and M2 was calculated using Equation (6) where I_D is $I_{D1,2}$ and k_n is a constant.

$$gm = \sqrt{2k_n \frac{W}{L} I_D} \tag{6}$$

The calculation of the size of the transistors M3, M4 and M5 was done by considering the input common mode ratio (CMR) where the transistors positioned to work in the saturation region, $V_{DS} > V_{GS} - V_{TH}$. Transistor M5 was set using Equation (7) and substitution of Equations (9) and (8).

$$I_{D5} = \frac{k_n}{2} \frac{W}{L} (V_{GS5} - V_{THN})^2 \tag{7}$$

$$I_{D1,2} = \frac{k_n}{2} \left[\frac{W}{L}\right]_{1,2} (V_{GS1,2} - V_{THN})^2 \tag{8}$$

$$CMR^+ = -V_{SS} - (V_{GS5} - V_{THN}) - V_{GS2} \tag{9}$$

Dimension calculation of transistors M3 and M4 was done using parameters CMR^- as Equation (10).

$$CMR^- = (VGS + VTHP)_4 - V_{DD} \tag{10}$$

By setting the value of $I_{D3} = I_{D4} = 2ID_2$, the dimension of M3 and M4 was then calculated using Equation (11).

$$\left[\frac{W}{2L}\right]_{3,4} = \frac{I_{D3,4}}{\frac{k_p}{2}(V_{GS3,4} + V_{THP})^2} \tag{11}$$

The current flow through the transistors M6 and M7, I_{D6} and I_7 was equal. They are calculated as Equation (12).

$$I_{D6,7} = SR(C_C + C_L) = 2\left(1 + \frac{C_L}{C_C}\right) I_{1,2} \tag{12}$$

In calculating the dimensions of transistor M7, $V_{GS5} = V_{GS7}$ and $I_{D7} = I_{D6}$ were set as stated in Equation (12). The size of W and L of transistor M7 was calculated as Equation (13) while M6 was calculated as Equation (14).

$$\left[\frac{W}{L}\right]_7 = \frac{I_{D7}}{\frac{k_n}{2}(V_{GS7} - V_{THN})^2} \tag{13}$$

$$\left[\frac{W}{2L}\right]_6 = \frac{I_{D6}}{\frac{k_p}{2}(V_{GS6} + V_{THP})^2} \tag{14}$$

The paired transistors, M8 and M5 act as current mirrors, and their dimensions are calculated based on Equation (15).

$$\frac{I_5}{I_{REF}} = \frac{\left[\frac{W}{L}\right]_5}{\left[\frac{W}{L}\right]_8} \tag{15}$$

Transistors M9 and M10 were selected from PMOS transistors that function as active resistors. Both transistors were made of the same size. The voltage across the two transistors was simply calculated by using the Kirchoff voltage law $-V_{DD}+V_{DS10}+V_{DS9}+V_{DS8}-V_{SS} = 0$ and $V_{DS9} = V_{DS10}$.

Up to this point, all the components used to construct the LDO (the error amplifier section, the pass transistor and the feedback resistors) have been obtained as seen in Figure 4.

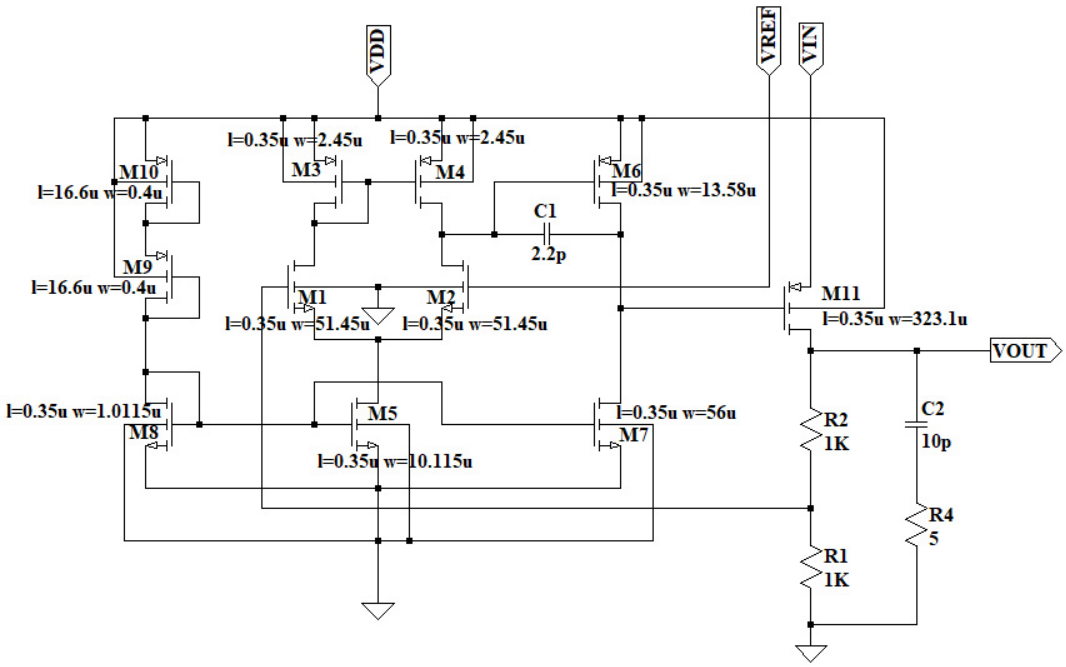
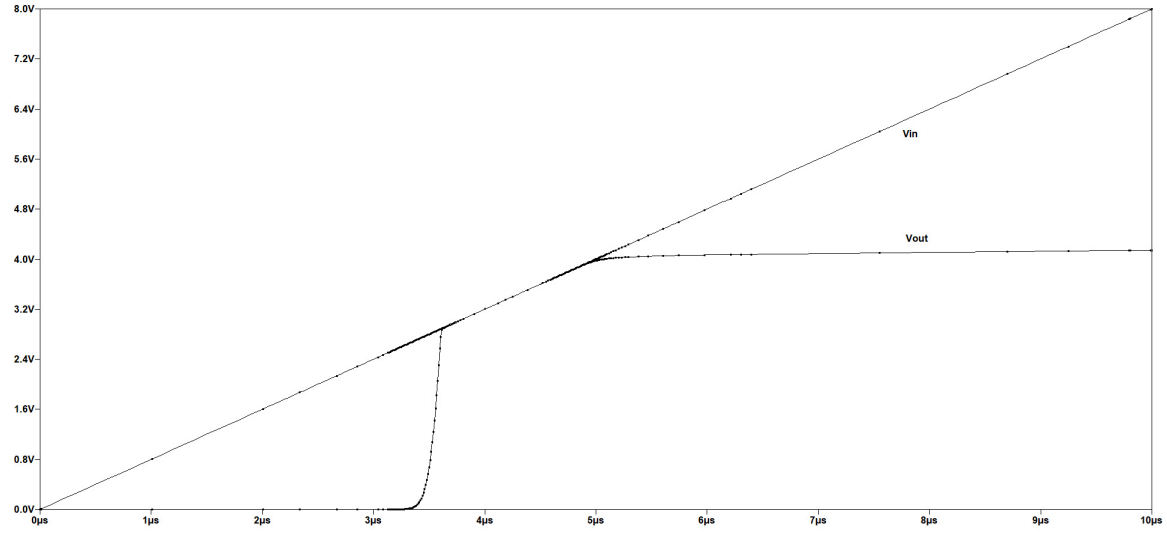


FIGURE 4. Designed LDO schematic

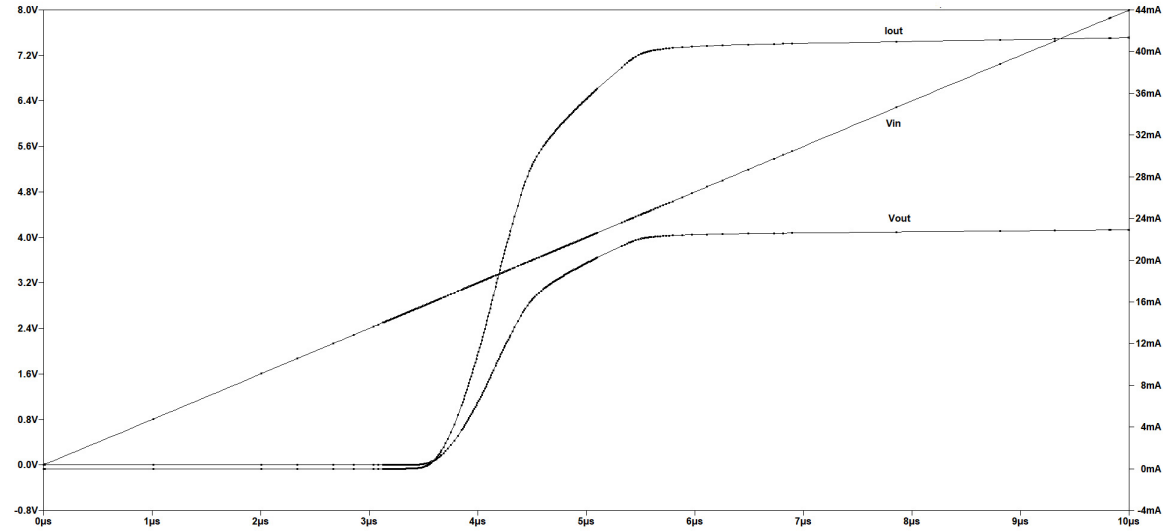
4. **Simulation Result.** After all supporting component values obtained, the next step was to simulate the main support block (OTA) and merge them into LDO circuit. Simulation was conducted using LTSPICE and its 0.35 μm library. The simulation result of the OTA's offset swing notices that OTA's ICMR was at −3.3 V to 3 V while the OTA's output was 0 V. The OTA designed also had the unity gain at 24 MHz and a phase margin of 55° to confirm its stability. This unity gain was enough to ensure the amplification of the LDO would not decrease since the frequency of the signal that was fed into the LDO was smaller than 24 MHz.

LDO simulation was performed after connecting all supporting blocks to form the LDO circuit according to the topology shown in Figure 3(a). As shown in Figure 5(a), at the unloaded condition, when the input was in the range of 3 V to 4 V, the output also marked the same voltage value. At the input voltage greater than 4 V, LDO started working to regulate a stable output voltage at 4 V.

To confirm the ability of the LDO at serving the load, a resistive load was attached at the output of the LDO in the simulation. The variable resistive load that was added was initiated from 100 Ω and continued to be lowered to 40 Ω. The simulation result of loaded



(a)



(b)

FIGURE 5. LDO simulation result: (a) No load; (b) 100 Ω

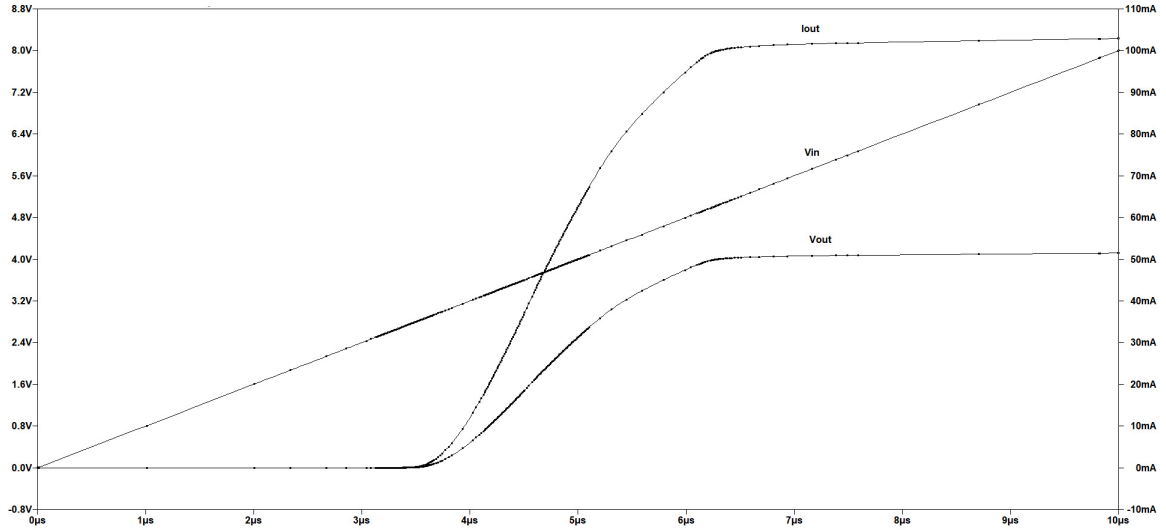


FIGURE 6. LDO with 40 Ω load simulation result

LDO can be seen at Figures 5(b) and 6. At 100 Ω load, the LDO began to regulate the output voltage to 4 V when the input voltage reached 4.5 V in 4.5 µS. However, if the load was lowered to 40 Ω, the regulated output 4 V and 100 mA current reached when the input voltage at 5 V. This regulated output voltage was obtained in 6.3 µS.

5. **Conclusion.** The LDO using operational transconductance amplifier has been designed. At 4.5 V of the supply voltage, the LDO designed is able to regulate the output voltage at 4 V to supply a maximum current of 100 mA to 40 Ω as the minimum load. The regulation voltage increases from 100 mV to 500 mV as the load decreases from no load (∞ Ω) to 40 Ω. The designed LDO is suitable for regulating the charging voltage for mobile phone's battery.

As future work, the LDO will be combined with other parts of power management and CMOS micro solar cell to be made into a chip that can be applied to mobile phone battery charging systems that use sunlight as its power source.

Acknowledgment. This paper is supported by DRPM Ministry of Education and Culture of The Republic of Indonesia Contract number: 309/E4.1/AK.04.PT/2021, July 12, 2021. The authors also gratefully acknowledge the helpful comments and suggestions of the reviewers, which have improved the presentation.

REFERENCES

[1] K. N. H. Ono and N. Nakano, A design of CMOS on-chip photovoltaic device and regulated DC-DC converter for micro system, *SASIMI 2013 Proceeding*, pp.25-27, 2013.

[2] D. K. K. Nomura and N. Nakano, Design of photovoltaic device and DC-DC converter on single chip using 0.18 µm standard CMOS tecnology, *Analog Integrated Circuit and Signal Processing*, no.78, pp.3-9, 2014.

[3] C.-H. Huang, Y.-T. Ma and W.-C. Liao, Design of a low-voltage low-dropout regulator, *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, vol.22, no.6, pp.1308-1313, 2014.

[4] M. Ferri, D. Pinna, E. Dallago and P. Malcovati, A 0.35 µm CMOS solar energy scavenger with power storage management system, *Research in Microelectronics and Electronics*, pp.88-91, DOI: 10.1109/RME.2009.5201369, 2009.

[5] Q. I. Ali, Design & implementation of a mobile phone charging system based on solar energy harvesting, *2010 1st International Conference on Energy, Power and Control (EPC-IQ)*, pp.264-267, 2010.

[6] S. Heng, *Research on High Performance LDO Regulator Operating with Low Power and Low Supply Voltage*, Ph.D. Thesis, University of Electro-Communication, 2009.

[7] C. Desai, D. Mandal, B. Bakkaloglu and S. Kiaei, A 1.66 mV FOM output cap-less LDO with current-reused dynamic biasing and 20 ns settling time, *IEEE Solid-State Circuits Letters*, vol.1, no.2, pp.50-53, 2018.

[8] D. K, H. V. Manjunath and K. A. Gupta, Design of CMOS LDO regulator in LTspice using Miller compensation method, *International Research Journal of Engineering and Technology (IRJET)*, vol.7, 2020.

[9] H. M. García, Low drop-out voltage regulator as a candidate topology for photovoltaic solar facilities, *Renewable Energy & Power Quality Journal*, pp.1-6, 2015.

[10] H. M. García, LDO-assisted DC/DC converters for power management integrated systems, *Proceedings of the Energy*, pp.1-6, 2017.

[11] H. L. M. Al-Shyoukh and R. Perez, A transient-enhanced low-quiescent current low-dropout regulator, *IEEE Journal of Solid-State*, vol.42, no.8, 2007.

[12] S. A. Z. Murad, A. Harun, M. N. M. Isa, S. N. Mohyar, R. Sapawi and J. Karim, Design of CMOS low-dropout voltage regulator for power management integrated circuit in 0.18-μm technology, *AIP Conference Proceedings*, vol.2203, no.1, https://aip.scitation.org/doi/abs/10.1063/1.5142098, 2020.

[13] J. Choi, J. Park, W. Jeong, J. Lee, S. Lee, J. Yoon, J. Kim and J. Choi, Design of LDO linear regulator with ultra low-output impedance buffer, *2009 International SoC Design Conference (ISOCC)*, pp.420-423, 2009.

[14] C. Ashwin, Design of a low voltage, low drop-out (LDO) voltage CMOS regulator, *International Journal of Scientific & Engineering Research*, vol.3, no.9, pp.40-45, 2012.

[15] P. Jainapur and C. R. Sharma, Modeling and design of a CMOS low drop-out (LDO) voltage regulator, *International Journal of VLSI and Embedded Systems (IJVES)*, vol.4, 2013.

[16] H. Afandi, *Design of Pipeline Analog to Digital Converter Based on CMOS Technology Embedded with Sensor for High Speed Camera Application*, Ph.D. Thesis, University of Gunadarma, 2009.

[17] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 4th Edition, Wiley-IEEE Press, 2019.

[18] J. Purnomo, E. P. Wibowo, B. Soerowirdjo, D. Nur'ainingsih and R. K. Harahap, Design of 100 MHz asynchronous pipeline ADC with N-comparator topology, *ICIC Express Letters, Part B: Applications*, vol.12, no.2, pp.99-109, 2021.

[19] M. Cermak, *Design of Low-Dropout Voltage Regulator*, Master Thesis, Czech Technical University, Prague, 2016.

[20] D. Nur'ainingsih, J. Purnomo, E. Wibowo, R. Harahap and B. Soerowirdjo, Design of accumulator dump for RFID readers using 0.35 μm CMOS technology, *Journal of Theoretical and Applied Information Technology*, vol.98, no.20, pp.3249-3259, 2020.

[21] J. Tang, C. Zhan, G. Wang and Y. Liu, A 0.7 V fully-on-chip pseudo-digital LDO regulator with 6.3 μA quiescent current and 100 mV dropout voltage in 0.18-μm CMOS, *IEEE the 44th European Solid State Circuits Conference (ESSCIRC2018)*, pp.206-209, 2018.