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DESIGN OF A BIPOLAR CASCADE VOLTAGE-DOUBLER FOR A NON-THERMAL FOOD PROCESSING SYSTEM USING UNDERWATER SHOCKWAVE

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Abstract. *Non-thermal food processing technology is receiving a lot of attention, because it can provide food without the destruction of nutrients. Among others, the processing with an underwater shockwave can reduce costs because it requires only some circuitry and electrodes, while other methods require using such as cold plasma and UV-light. In this study, we suggest a new voltage multiplier that is a part of the underwater shockwave system. Unlike conventional Cockcroft-Walton type multipliers, the proposed multiplier has a bipolar cascade voltage-doubler topology. The proposed multiplier is theoretically analyzed and simulated. The theoretical analysis provides design guidance, which can help future circuit designers. Furthermore, in the experiment, the measured charging time for the proposed voltage multiplier's output capacitor is shortened from 220 seconds (the conservative) to 158 seconds. The experiment confirms the underwater shockwave system's feasibility with the proposed voltage multiplier for non-thermal food processing.*
Keywords: Non-thermal food processing, Underwater shockwave, Voltage multiplier, Circuit model, Design guidance

1. **Introduction.** Heating food has been a typical way of food processing technologies, while this way can destroy its nutrients such as vitamins and polyphenols [1]. As a desire for people's nutritious meals increases, non-thermal food processing technologies have drawn interest from them [2]. Representative non-thermal food processing methods researched in the past are as follows: high voltage arc discharge [3,4], cold plasma [5,6], UV-light [7,8], low temperature [9], high hydrostatic pressure [10], and underwater shockwave [11-15]. Among these methods, the underwater shockwave costs the lowest and can provide users with non-destroyed food ingredients. Simply explaining the non-thermal food processing operation with underwater shockwaves, its output capacitor charged by a high voltage over 3 kV generates a shockwave in water to process a target food. Therefore, to improve the system's performance, we focus on the high voltage generating circuit of the food processing system. In the underwater shockwave system, previous studies utilize inductor-less voltage multipliers such as Cockcroft-Walton topology [16] to reduce the system's volume and cost. However, the multipliers' charging time increases proportionally to the number of multiplier stages consisting of capacitors and electrical switches because the higher stepped-up voltages a target system requires, the bigger number of multiplier stages it should be set up. To solve this problem, the series-connected Cockcroft-Walton multiplier [11,12] and its families [13-15] have been proposed in past studies. In these high voltage multipliers, a high voltage gain is achieved by converting an input voltage twice by several Cockcroft-Walton multipliers. However, there is still room for improvement in the voltage gain.

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In this study, a new voltage multiplier is suggested to improve the conservative circuit with the problems abovementioned. Unlike the conventional Cockcroft-Walton type multipliers [11-16], the proposed multiplier has a bipolar cascade voltage-doubler topology. By cascading bipolar voltage-doublers, the proposed circuit can achieve high voltage gains with small number of multiplier stages. The proposed circuit is analyzed theoretically and simulated to verify its performance. Next, the suggested voltage multiplier is superimposed to a prototype of the underwater shockwave non-thermal food processing unit. Using a target food, we evaluate the food processing system's effectiveness with the suggested voltage multiplier. The rest of this paper is structured as follows. Section 2 describes and analyzes the new voltage multiplier. In Section 3, the suggested voltage multiplier is utilized for the prototype and shows the processed food. Section 4 concludes this study.

2. **Voltage Multiplier.**

2.1. **Circuit configuration.** Figure 1 shows the suggested voltage multiplier. The voltage multiplier consists of 24 capacitors and 24 diodes, an input source, and two output ports. Table 1 lists the details of circuit components of two voltage multipliers. The proposed voltage multiplier reduces the number of circuit components, comparing it with that of the conservative [11,12].

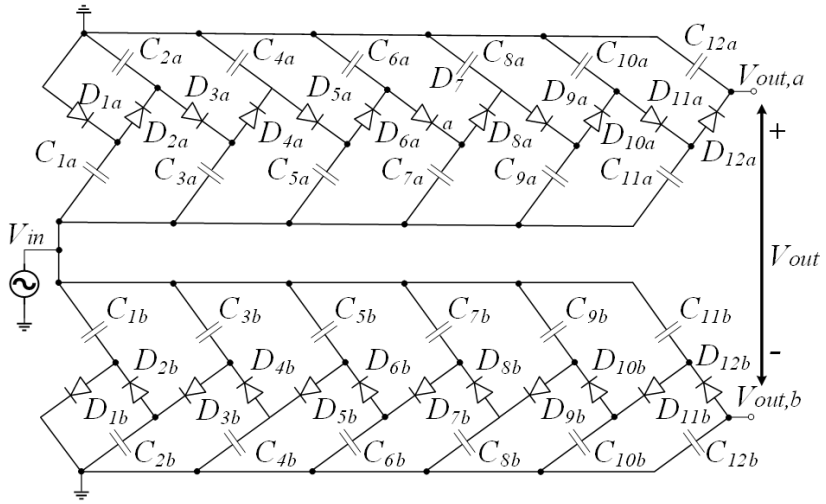


FIGURE 1. The proposed voltage multiplier

TABLE 1. Comparison of component counts

	[11,12]	Proposed voltage multiplier
Capacitor	48	24
Diode	52	24
Total	100	48

2.2. **Theoretical analysis.** The proposed voltage multiplier is modeled based on KCL and KVL (Kirchhoff's current and voltages law), FE model (Four-terminal equivalent circuit model), and SSL (Slow switching limit) and FSL (Fast switching limit) model. This analysis focuses on the operation of the proposed voltage multiplier in its stable state, where it neglects the ripple voltages of capacitors. Two modelings are conducted with instantaneous circuits during state-1 and 2, as shown in Figure 2.

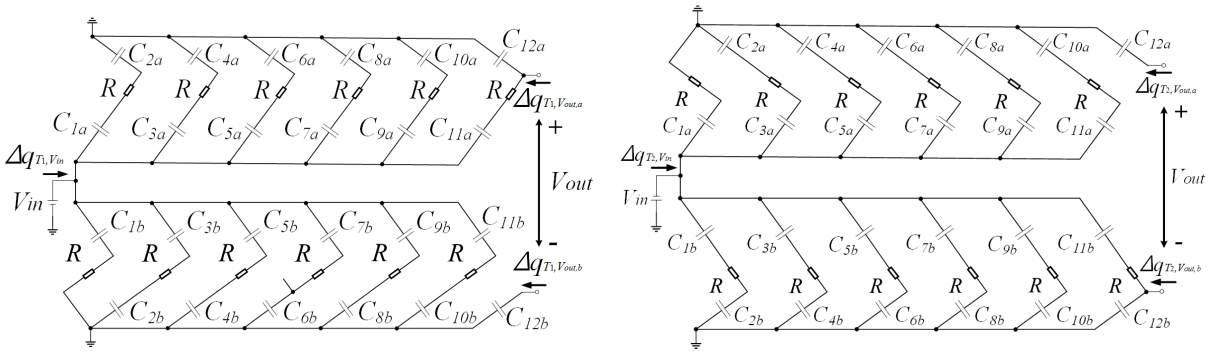


FIGURE 2. Instantaneous equivalent circuit: (a) State-1 and (b) state-2

The first step of the analysis is to model the instantaneous circuits by using the FE model. From this model, the ideal current and voltage conversion ratio and the relations of them are derived. In the lower block during state-1 and 2, the charge amounts of capacitors, inputs, and outputs can be expressed from KCL as (1), neglecting those of the upper block.

$$\begin{aligned} &\text{State-1: } \Delta q_{T_1,v_{in}} = \sum_{x=1}^{11} \Delta q_{T_1}^{xb} \ (x = \text{ odd numbers}),\ \Delta q_{T_1,v_{out,b}} = \Delta q_{T_1}^{12b} - \Delta q_{T_1}^{11b} \\ &\text{State-2: } \Delta q_{T_2,v_{in}} = \sum_{x=1}^{11} -\Delta q_{T_2}^{xb} \ (x = \text{ odd numbers}),\ \Delta q_{T_2,v_{out,b}} = \Delta q_{T_2}^{12b} \end{aligned} \tag{1}$$

where $\Delta q_{T_1,v_{in}}$ and $\Delta q_{T_2,v_{in}}$ are the charge amounts of inputs, $\Delta q_{T_1,v_{out,b}}$ and $\Delta q_{T_2,v_{out,b}}$ are those of outputs of the lower block, $\Delta q_{T_1}^{xb}$ and $\Delta q_{T_2}^{xb}$ are those of the x-th capacitor in the lower block during state-1 and 2, respectively. Practically, the input source charges the capacitors of the upper block, but this modeling uses the superposition principle. Average input and output charge amounts of the lower block during an operation cycle of state-1 and 2 are given (2)

$$\Delta q_{v_{in}} = 2 \times \Delta q_{T_1,v_{in}},\ \Delta q_{v_{out,b}} = -\Delta q_{T_1}^{11b} \text{ and } \Delta q_{v_{out}} = -12\Delta q_{v_{out,b}} \tag{2}$$

where $\Delta q_{v_{in}}$ and $\Delta q_{v_{out}}$ are the charge amounts of the input and the output of the lower block, neglecting those of the upper block. Using (2), the input and output voltage and current of the lower block as (3) can be calculated with the period of an operation cycle, T.

$$I_{in} = \frac{\Delta q_{v_{in}}}{T} = -12 I_{out,b} \text{ and } V_{out,b} = 12 V_{in} \tag{3}$$

where the relation between the input and output current and voltage of the lower block can be derived from the fact that the FE model has an ideal transformer. From the symmetric structure, the total output voltage between the upper and the lower block is yielded as (4).

$$V_{out} = 24 V_{in} \tag{4}$$

The second step is to analyze the instantaneous circuits by using the SSL-FSL model. This modeling is conducted with the relations of the charge amounts of capacitors in the circuits. The model yields some charge multiplier vectors and the output resistance of the proposed multiplier. As shown as (1) and (2), the charge amounts of the capacitors can be expressed by using the charge amount of the output. The charge multiplier vectors of the lower block of the circuits, a_c^1 and a_c^2 during one operation cycle can be derived as (5).

$$a_c^1 = \begin{bmatrix} -1 & -1 & -1 & -1 & -1 & -1 & -1 \end{bmatrix}^T \text{ and } a_c^2 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}^T \tag{5}$$

where a_c^x is the charge multiplier vector of the lower block of state-x. Using the derived vectors, the output resistance, R_{out}, is calculated as (6).

$$R_{out} = 2 \times \sqrt{R_{SSL}^2 + R_{FSL}^2} = 2 \times \sqrt{\left(\frac{22}{2C_i f}\right)^2 + (44R)^2} \tag{6}$$

where R_{SSL} and R_{FSL} are the output impedance for the slow and fast switching limit, C_i is the capacitance of capacitors, f is the operation frequency, and R is the diode series resistance. The reason for two times the output resistance is that $\sqrt{R_{SSL}^2 + R_{FSL}^2}$ is that of the lower block, and the proposed voltage multiplier has its symmetric structure. A circuit model of Figure 3 [17] describes the results of the two modelings, where m is the conversion ratio. In the final model, the turn ratio (the value is 24) of the ideal transformer is from the FE modeling, and the output resistance is from the SSL and FSL modeling.

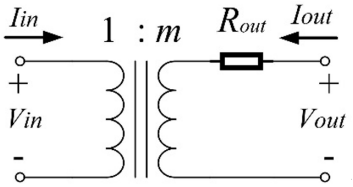
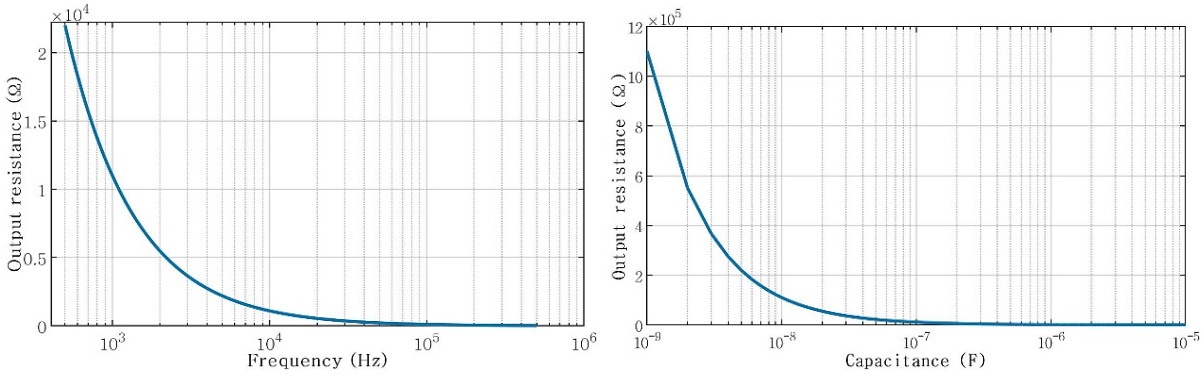


FIGURE 3. Circuit model for the proposed voltage multiplier

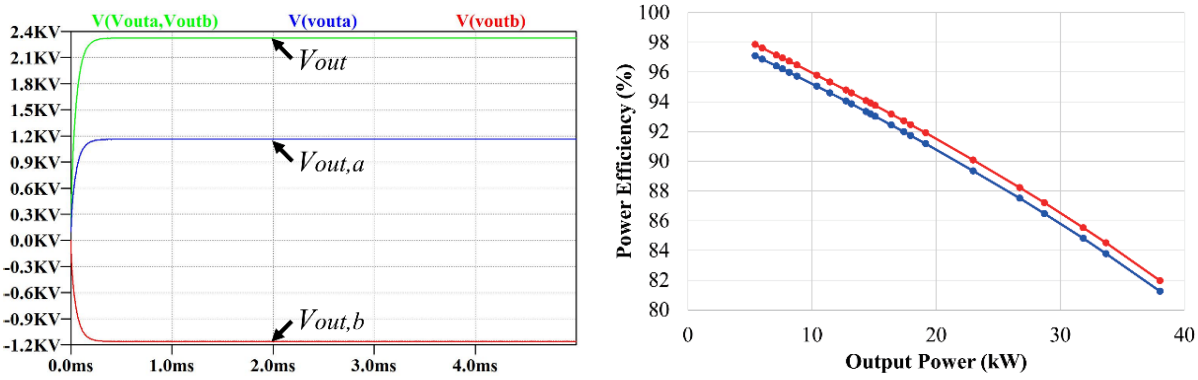
2.3. **Components selection.** In this subsection, the optimization is implemented by tuning the target components' values and fixing others. From doing this, one can examine the output resistance regulations. The first parameter is operation frequency. Figure 4(a) plots the output resistance regulation at different frequencies from 500 Hz to 10 kHz, where the capacitance is 1 μF, and R is 0.01 Ω. The regulation curve indicates that the higher the frequency is, the smaller the output resistance is. However, considering the maximum frequency with the diodes' recovering time and capacitors' charging time, one has to select a proper operation frequency for the voltage multiplier. The second parameter is capacitance. Figure 4(b) shows the curve of the output resistance regulation at different capacitances from 10 nF to 10 μF. The other parameters' values are as follows. The operation frequency is 10 kHz and R is 0.01 Ω. The curve in Figure 4(b) demonstrates that the output resistance decreases as the capacitance increases. In the same manner as selecting the proper frequency, there is an upper limit of the capacitance. A proper capacitance for the proposed voltage multiplier can be set up from the analysis of the simple RC circuit of the instantaneous circuits and the SSL-FSL modeling result. Taking 10 μF of the capacitance, for example, the time constant is 50 sec, and the output resistance is 110 Ω. Given that the time constant is 0.05% of the one operation period, 10 μF can be a proper capacitance for the voltage multiplier.

2.4. **Simulation.** The proposed voltage multiplier is simulated with circuit parameters as followed: +100 VDC and −100 VDC, R is 0.05 Ω, f is 1 MHz, and R_L is from 100 Ω to 1 kΩ. By comparing the simulated and the modeled (calculated) results, the accuracy of the theoretical analysis is verified. The range of the simulated output power is from 5 kW to 40 kW. Figure 5(a) plots the output voltage at 15 kW of the output power. Figure 5(b) shows the simulated and calculated power efficiencies at different output powers. The simulated power efficiencies are about 0.73% higher than those of the calculated, on average. This comparison confirms that the design methodology implemented in previous subsections is reliable.



(a) (b)

FIGURE 4. Modeled output resistance regulation: (a) For frequency and (b) for capacitance



(a) (b)

FIGURE 5. Simulation and comparison: (a) Simulated output voltage at 6 kW and (b) simulated and calculated power efficiencies at different output powers

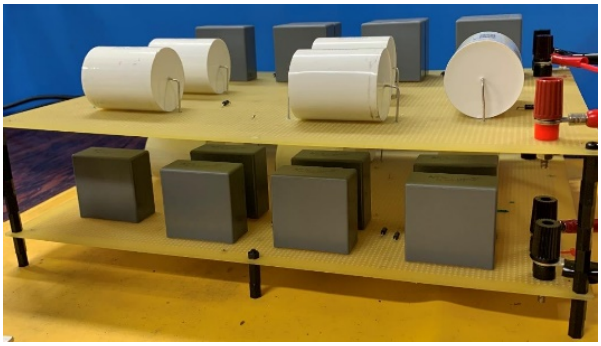


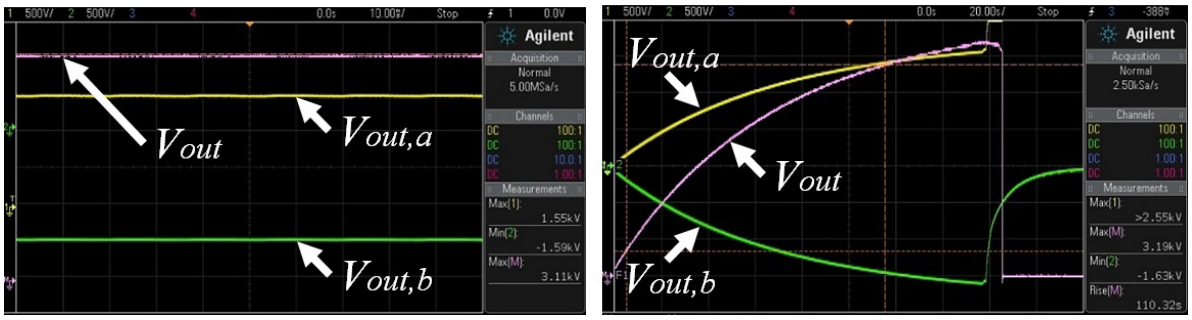
FIGURE 6. Experimental proposed voltage multiplier

3. **Experiment.**

3.1. **Experiment environment.** To evaluate the proposed voltage multiplier, the proposed is applied to an experimental prototype of the underwater shockwave non-thermal food processing unit. Figure 6 shows the experimental proposed voltage multiplier. The transformer and the rectifier step down and rectify the whole system input (100 VAC/60 Hz). The driver circuit controls the input of the proposed. The rectified and boosted output voltage charges the output capacitor. The details of the circuit components are

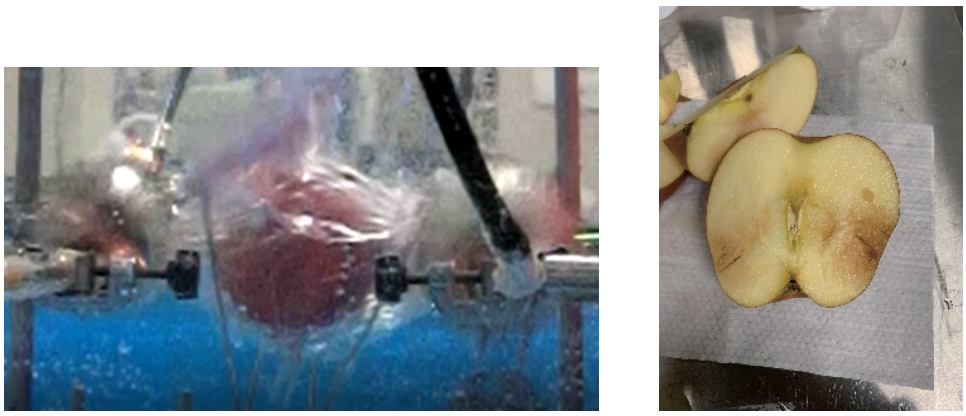
as follows: Rectifier (1N4007, 33 μF), input driving circuit (PIC12F1822, AQW2163), and output capacitor (200 μF). In the operation of the prototype, the proposed voltage multiplier charges the output capacitor. A discharging of the charged capacitor through the electrodes can generate a shockwave to process a target food.

3.2. **Experiment result.** Figure 7(a) shows the measured output voltage of the proposed voltage multiplier. The yellow and green waveforms are the upper and the lower blocks output voltages, respectively. The waveforms confirm that two output voltages charge the output capacitor by about 3 kV (the pink waveform in Figure 7(b)). While the conservative voltage multiplier of [11,12] requires about 220 seconds to fully charge its output capacitor, the proposed takes about 158 seconds shown in Figure 7(b). We select an apple as a target food. The apple wrapped in a zipper back is set up in the experimental food processing unit's water tank shown in Figure 8(a). Figure 8(b) demonstrates the cross-section of the processed target food. Figure 8(b) certifies that the experimental food processing unit can completely crush the flesh of the target food located near the electrodes.



(a) (b)

FIGURE 7. Measured results: (a) Output voltage and (b) rise time



(a) (b)

FIGURE 8. Measured results: (a) Discharging process and (b) cross-section of the apple

4. **Conclusions.** This study suggests a new voltage multiplier that can be applied to a non-thermal food processing system using an underwater shockwave. The proposed voltage multiplier reduces its circuit components. This reduction can improve a safety issue of the conservative voltage multiplier that unbalanced charging of multiple capacitors can cause. The theoretical analysis for the proposed voltage multiplier can provide design

guidance for selecting the operation frequency and the capacitance. The analysis results are verified by comparing them with the simulated results. The guideline can help future circuit designers set up a proper range of circuit parameters. The result of the experiment with the prototype of the non-thermal food processing unit reveals as follows. 1) The required time for the proposed voltage multiplier to charge the output capacitor is shorter than that of the conservative. 2) The prototype can generate the underwater shockwave to soften the target food. This experiment can prove the feasibility of the non-thermal food processing system with the proposed voltage multiplier. In a future study, we are going to investigate the dynamic currents of the proposed voltage multiplier to clarify the effect of underwater shockwaves.

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