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DIGITAL FREQUENCY-LOCKED LOOP BASED ON DOUBLE-EDGE COUNTER

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Abstract. *In the clock generator for clock distribution for driving each system of the mobile communication device, it is desirable to quickly recover from the stopped state and to supply a stable clock from the viewpoint of low power consumption. In this paper, we propose digital frequency-locked loop (DFLL) based on double-edge counter. In this circuit, the frequency detection error between the input signal and the output signal can be reduced by half compared to the conventional DFLL. The steady-state frequency error of the output signal can also be reduced by half. Accordingly, when the frequency error characteristic in the steady-state is set to be the same as that of the conventional DFLL, the upper limit frequency of the lock-in range can be doubled. Moreover, the pull-in time and cycle slip control inherit the characteristics of the DFLL that we previously proposed.*
Keywords: Frequency-locked loop, Double-edge, Frequency detection error, Phase control, PLL

1. **Introduction.** In Society 5.0, advanced fusion of cyber space and physical space is required. Among them, mobile communication devices are playing an increasingly important role in transferring various types of information from physical space to cyber space. In addition to a clock signal generator that drives itself, a microprocessor incorporated in a mobile communication device has a plurality of clock signal generators for distributing clocks for driving other circuits on the system, and it is synchronized with the external system. In the mobile communication device, since the standby-state is extremely long, the power consumption in that state greatly affects the power consumption of the entire system from the viewpoint of the battery life. Therefore, if it is possible to stop the clock generation circuit during standby and stop the clock supply to the system, not only the power consumption of each system, but also the power consumption related to the clock signal generator can be reduced [1,2]. However, when the system returns from the standby state, the quick supply of the clock signal becomes a very important matter which affects the performance of the entire system.

One of the commonly used circuits in clock signal generators is a phased-locked loop (PLL). However, PLLs require frequency and phase lock from the time the input signal is added until the output clock is generated. Therefore, it takes some time for the output clock to stabilize, which makes it difficult to quickly recover from the system standby state. In order to shorten this time, the time constant of the filter constituting the loop

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may be set small, but there arises a problem that the jitter of the output signal increases [3-5].

On the other hand, a frequency-locked loop (FLL) is a clock signal generator which does not require the phase control. The FLL is a circuit that generates a clock locked only the frequency for the input signal, and the phase is not locked. Consequently, it is possible to shorten the time until clock generation compared to the PLL [6,7]. Therefore, when FLL is used as a clock generation circuit in a system, it can shorten the stability time of the system. However, since the conventional FLL has an analog configuration, there is a problem that an accurate frequency error between the input signal and the output signal cannot be detected. In addition, the use of FLL as a clock distribution circuit in a mobile communication device has a problem in terms of integration.

The authors previously proposed an all-digital FLL (DFLL) that realizes a very accurate output signal frequency to the input signal and fast initial pull-in [8]. This DFLL can complete the initial frequency pull-in in one cycle of the input signal. Even when a cycle slip occurs between the input signal and the output signal, a stable output signal can be obtained without being affected by the cycle slip. Next, the authors proposed DFLL, which solved the problem of falling into a pseudo-locked state in which the frequencies of the input and the output signals were locked while maintaining the relationship of 1: n (n is an integer excluding 1) [9]. This DFLL can also match the phase of the input signal and the output signal. However, the conventional DFLL that has been proposed is configured to control the loop using the rising edge of the reference clock. Therefore, the frequency error detection between the input and output signals had an error of less than one reference clock cycle. Since this error is directly related to the frequency error of the output signal, it has been necessary to improve the error for practical use.

In this paper, we propose the DFLL based on double-edge counter that improves the above problem. The proposed DFLL uses a double-edge counter that counts both edges of the reference clock as a counter constituting the circuit. Therefore, the proposed DFLL is possible to control in half cycle units of the reference clock, and the frequency detection error between the input signal and the output signal can be reduced to half compared to the conventional DFLL. The steady-state frequency error of the output signal is also reduced by half. Accordingly, when the frequency error characteristic in the steady-state is set to be the same as that of the conventional DFLL, the upper limit frequency of the lock-in range can be doubled. Furthermore, the pull-in time and cycle slip control have the same characteristics as the conventional DFLL.

In Chapter 2, we describe the basic operation in frequency error detection of the conventional DFLL. In Chapter 3, we describe the circuit configuration of the proposed DFLL and its basic operation analysis. In Chapter 4, we show the simulation results by Verilog-HDL. Finally, Chapter 5 is a conclusion.

2. Frequency Error Detection of Conventional DFLL.

Figure 1 shows the block diagram of the conventional DFLL. Figure 2 shows the operation waveforms in frequency error detection of the conventional DFLL. The conventional DFLL detects the error value by counting the number of reference clocks that pass between the frequency errors of the input signal and the output signal (time t_1 to t_3). Therefore, at the start of error detection, if the reference clock rises (time t_2) immediately after the frequency error signal is generated (time t_1), there will occur a detection error of less than one period of the reference clock. At the end of error detection, if the reference clock rises (time t_4) immediately after the frequency error signal falls (time t_3), a detection error similar to that at the start of error detection occurs. The conventional DFLL has a configuration in which a signal obtained by dividing the reference clock based on the detected value is fed back as an output signal. As a result, the detection error of the frequency error is directly generated as the frequency error of the output signal.

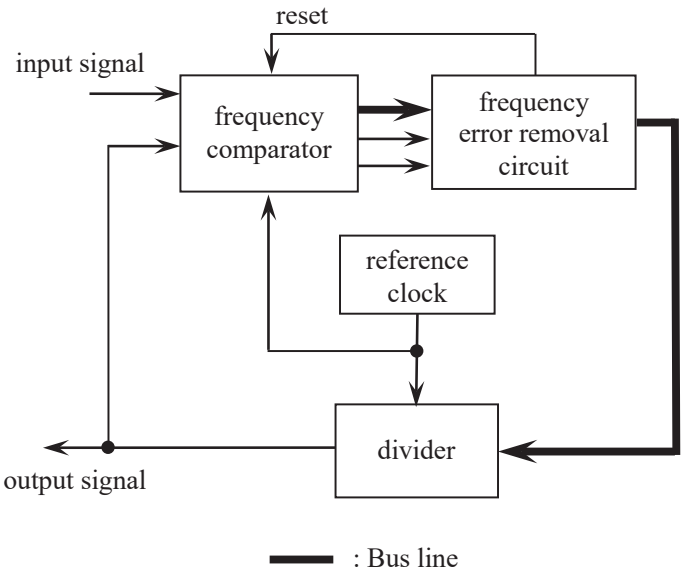

FIGURE 1. Block diagram of conventional DFLL

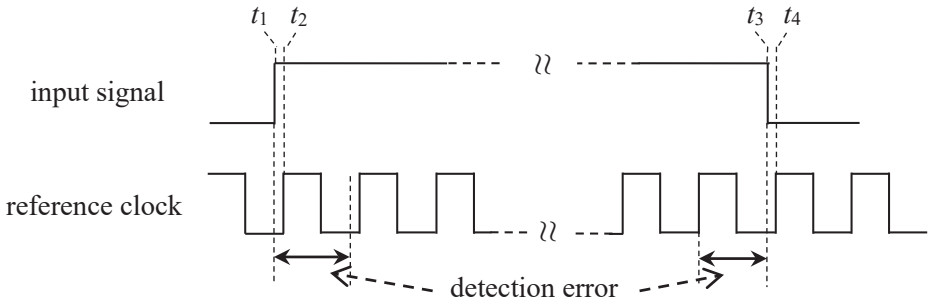

FIGURE 2. Waveforms for frequency error detection of conventional DFLL

On the other hand, for a frequency divider that generates an output signal, when a counter that counts only the rising edge of the reference clock is used, the output signal is controlled in units of one cycle of the reference clock. Hence, this has limited the reduction of the steady-state frequency error of the output signal.

3. Circuit Configuration and Operation Analysis of the Proposed DFLL.

3.1. **Circuit configuration of the proposed DFLL.** Figure 3 shows the block diagram of the proposed DFLL. T-FF1, T-FF2, T-FF3, EX-OR, logic gate, and U/D-counter constitute the digital frequency comparator. FER is an adjustment circuit for removing the frequency error between the input signal and the output signal generated from the digital frequency comparator. Divider is a variable frequency divider that divides the reference clock according to the value of FER and generates an output signal. fx is a reference clock source for controlling the loop. Also, U/D-counter in the digital frequency comparator and divider use a double-edge counter that counts both edges of the reference clock.

3.2. **Circuit configuration and operation of double-edge counter.** Figure 4 shows the circuit configuration of the double-edge counter used in the proposed DFLL and its operation waveforms. In order to count both edges of the input clock, two counters that separately count rising and falling edges may be used, and the count values may be added. However, in this configuration, when an adder is included, the circuit scale is more than

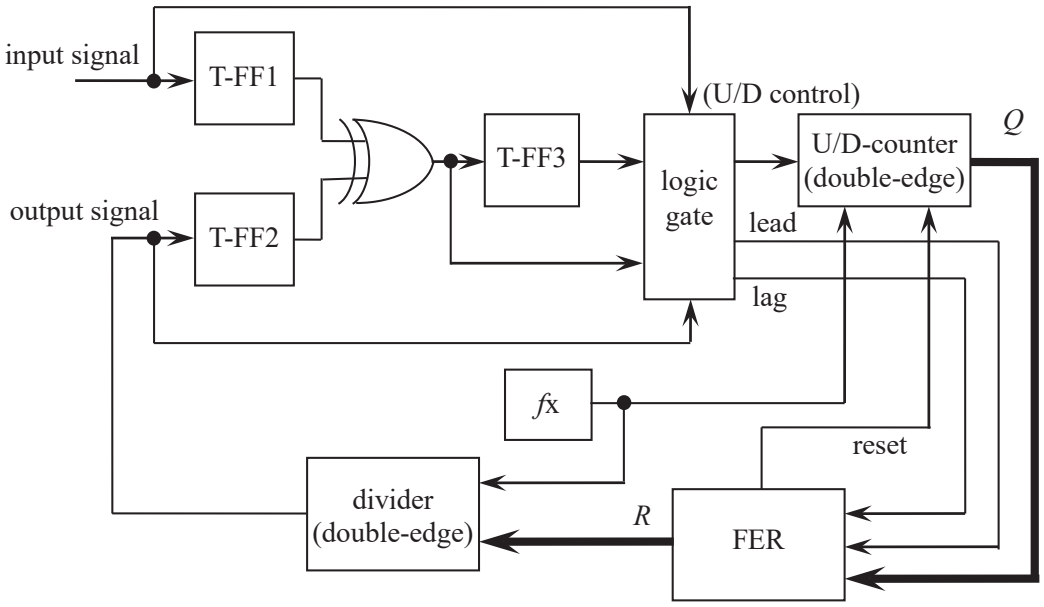

FIGURE 3. Circuit configuration of the proposed DFLL based on double-edge counter

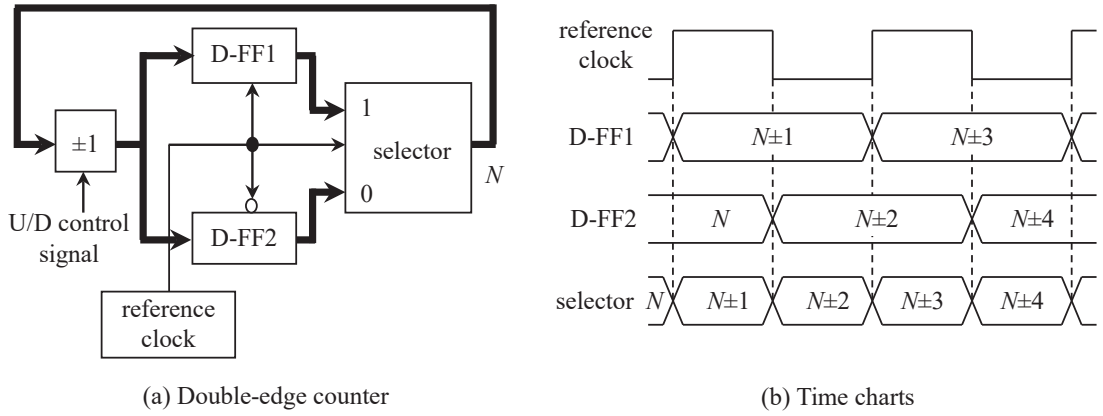

FIGURE 4. Circuit configuration of double-edge counter and its time chats

twice that of a single edge counting counter. Hence, this double-edge counter is configured to use a selector to count both edges.

In this circuit, the value "±1" for the output value "N" of the selector by the ±1 circuit controlled by the up/down signal from the logic gate is always input to two D-FFs. As shown in Figure 4(b), the value of "$N \pm 1$" is set to D-FF1 at the rising edge of the input clock and to D-FF2 at the falling edge. The selector selects the value of D-FF1 when the input clock is "1" and the value of D-FF2 when it is "0". As a result, the value of D-FF updated every half cycle of the input clock is output to the selector. Therefore, this double-edge counter can obtain an operation of counting up or down every half cycle of the input clock.

3.3. **Operational analysis of the proposed DFLL.** Figure 5 shows the waveforms of the proposed DFLL based on double-edge counter. At time t_1, when the input signal becomes high-level, the EX-OR that constitutes the digital frequency comparator outputs

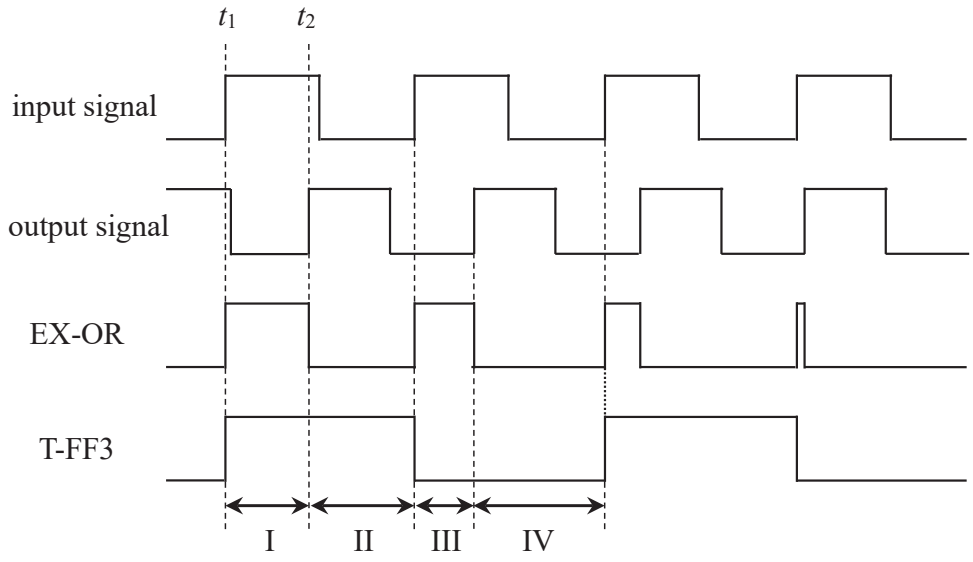

FIGURE 5. Waveforms of the proposed DFLL

a high-level. Next, when the output signal becomes high-level at time t_2, the EX-OR outputs a low-level. This output of EX-OR is divided by T-FF3.

Next, we explain the detection operation of frequency error. In the state I of Figure 5, the U/D-counter counts up both edges of the reference clock that pass while the output of EX-OR is at the high-level from the initial value "X". Assuming the both edges number (up-count value) of the reference clock passing while the state I is "Y", the count value "Q" of U/D-counter is "$X + Y$" at the end of state I.

In the state II, the count value "Q" is held.

In the state III, U/D-counter down-counts the reference clock number that passes while the output of EX-OR is at the high-level. Assuming the both edges number (down-count value) of the reference clock passing while the state III is "Z", the count value "Q" of U/D-counter is "$X + Y - Z$". As a result, the count value "Q" becomes a value corresponding to the frequency error between input signal and output signals at the end of state III.

In the state IV, the count value "Q" of U/D-counter is transferred to FER of the next stage. If the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y > Z$", FER decreases the output value which becomes the dividing ratio "R" of divider by the value corresponding to the frequency error. When the dividing ratio before state IV is "R_{pre}", the dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} - (Y - Z) \tag{1}$$

As a result, the output frequency of the proposed DFLL increases according to the difference between "Y" and "Z", so that it operates to remove the frequency error between input and output signals.

Conversely, if the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y < Z$", FER increases the output value by the value corresponding to the frequency error. The dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} + (Z - Y) \tag{2}$$

As a result, the frequency of the output signal of the proposed DFLL is lowered by the difference between "Y" and "Z", and the same operation is performed. At this time, the count value "Q" of the U/D-counter is reset to the initial value "X" to prepare for the next count.

Here, let us consider the frequency lock-in range and steady-state frequency error of the proposed DFLL. The proposed DFLL is configured to determine the frequency of the output signal by dividing both edges of the reference clock by the dividing ratio "R". Consequently, the frequency lock-in range is determined by the setting range of the dividing ratio "R". Here, when the lower limit value of the dividing ratio is "$R_{\min}$" and the upper limit value is "$R_{\max}$", the frequency lock-in range of the proposed DFLL is determined as follows.

$$\frac{2f_s}{R_{\max}} \leq f_{in} \leq \frac{2f_s}{R_{\min}} \tag{3}$$

where f_{in} is the frequency of input signal and f_s is the frequency of the reference clock.

Next, we consider the steady-state frequency error. The reference clock and the input signal of the proposed DFLL are not locked. In addition, the DFLL is a configuration that controls the frequency of an output signal by dividing a reference clock by the double edge counter. For this reason, since the frequency control of the proposed DFF is a unit of a half cycle of the reference clock, a steady-state frequency error that is less than the half of the reference clock at the maximum occurs in the output signal. Therefore, the average frequency f_{avg} of the output signal is expressed as follows.

$$f_{avg} = \frac{2f_s \cdot \left(\dfrac{1}{R} + \dfrac{1}{R \pm 1}\right)}{2} = 2f_s \cdot \left(\frac{1}{R} + \frac{1}{R \pm 1}\right) \tag{4}$$

In consequence, if the dividing ratio "R" is set to a certain large value, the influence on the jitter suppression effect by this error is considered to be negligible.

4. **Simulation Result.** This simulation was described using Verilog-HDL as hardware description language.

Figure 6 shows the simulation waveforms of each part of the conventional DFLL. The counter operation occurs immediately after the rise of the frequency error signal. Also, at the time of falling of the frequency error signal, the count is not operated. From this, it is found that the conventional DFLL generates a detection error of less than one cycle of the reference clock at the maximum depending on the timing of the input signal and the reference clock.

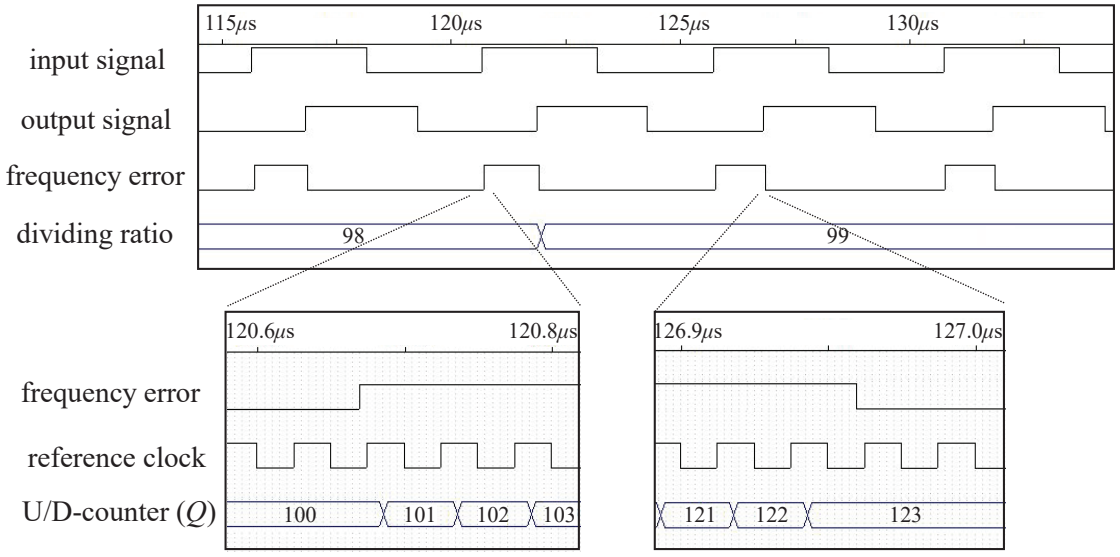

FIGURE 6. Simulation waveforms of conventional DFLL

Figure 7 shows the simulation waveforms of each part of the double-edge counter. From this, since this circuit counts up or down every half cycle of the input clock, it is found that it operates as the double-edge counter.

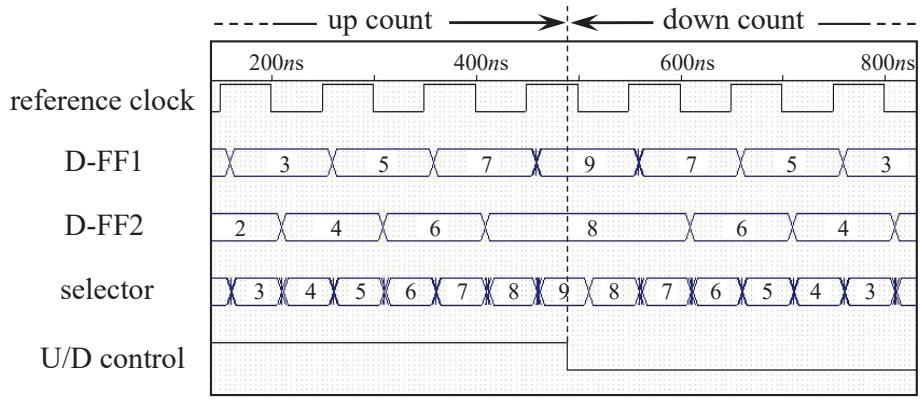

FIGURE 7. Simulation waveforms of double-edge counter

Figure 8 shows the simulation waveforms of each part of the proposed DFLL based on double-edge counter. From this, since the count operation occurs within half the period of the reference clock with respect to the frequency error signal, it is found that the detection error can be reduced to 1/2 compared to the conventional DFLL.

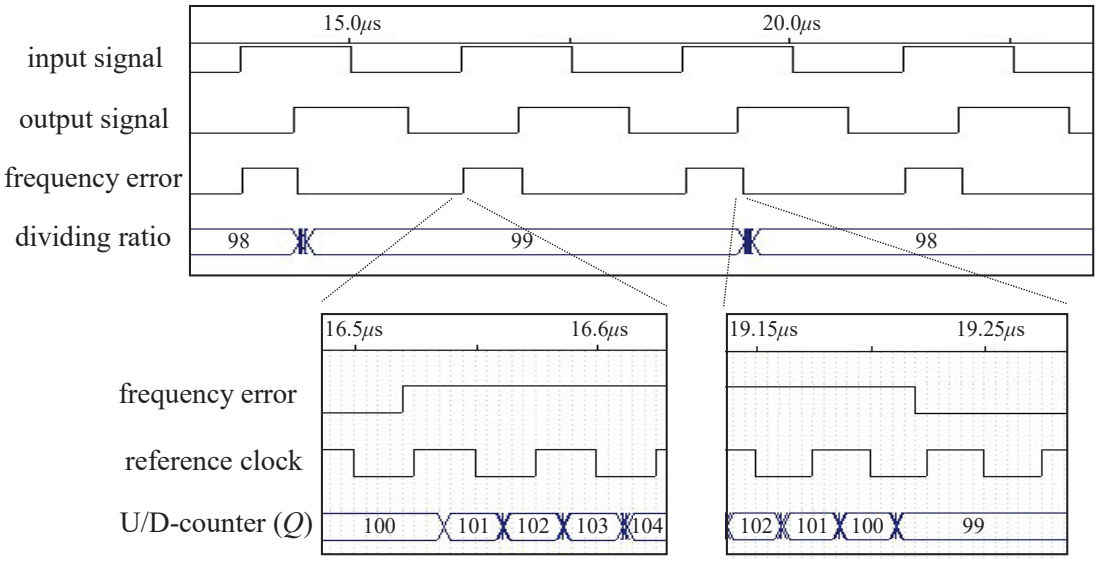

FIGURE 8. Simulation waveforms of the proposed DFLL

In addition, it was confirmed by simulation that the lock-in range and the steady-state frequency error of the proposed DFLL operate within the range satisfying Equations (3) and (4). Moreover, it was also confirmed that the upper limit frequency of the lock-in range is doubled when the steady-state frequency error characteristic is set to be the same as that of the conventional DFLL.

5. **Conclusion.** In this paper, we proposed the DFLL based on double-edge counter that enables control of the reference clock in half-cycle units. This DFLL was able to reduce the frequency detection error and the steady-state frequency error of the input and the

output signals by half compared with the conventional DFLL. Also, when the steady-state frequency error characteristic was set to be the same as that of the conventional DFLL, the upper limit frequency of the lock-in range could be doubled. Moreover, it was confirmed that the pull-in time and the cycle slip characteristics were the same as those of the conventional DFLL.

In the future, we plan to examine the configuration to further reduce the frequency detection error and the steady-state frequency error.

REFERENCES

[1] Y. Harada, K. Fujimoto, K. Eguchi, M. Fukuhara and M. Yoshida, A wide range manhattan distance search circuit using neuron CMOS inverters, *International Journal of Innovative Computing, Information and Control*, vol.14, no.1, pp.161-170, 2018.

[2] M. Miyazaki and K. Ishibashi, A 3-cycle lock time delay-locked loop with a parallel detector as a low-power system-clock generator, *IEICE Trans. Electronics*, vol.J83-C, no.6, pp.502-508, 2000.

[3] J. R. Cessna, Steady state and transient analysis of a digital bit synchronization phase locked loop, *Int. Conf. Rec. IEEE Int. Conf. Commun.*, 1970.

[4] J. R. Cessna and D. M. Levy, Phase noise and transient times for a binary quantized digital phase-locked loop in white Gaussian noise, *IEEE Trans. Commun.*, vol.20, no.2, pp.94-104, 1972.

[5] F. Sato, T. Saba, D. Park and S. Mori, Digital phase-locked loop with a wide locking range using fractional divider, *IEICE Trans. Commun.*, vol.J78-B-I, no.1, pp.86-93, 1995.

[6] D. F. Stout, *Handbook of Operational Amplifire Circuits Design*, McGraw-Hill, 1976.

[7] K. Tanaka, A. Hyogo and K. Sekine, A frequency synthesizer using a frequency locked loop, *IEICE*, vol.CAS89-64, pp.73-78, 1989.

[8] M. Yahara, K. Fujimoto, Y. Harada and K. Matsumoto, A 2-mode digital FLL using frequency comparator corresponding to cycle slip, *ICIC Express Letters, Part B: Applications*, vol.8, no.9, pp.1271-1278, 2017.

[9] M. Yahara, K. Fujimoto and D. Nishiguchi, A reset type 2-mode digital FLL with anti-pseudo-lock function and phase control, *ICIC Express Letters, Part B: Applications*, vol.10, no.10, pp.903-910, 2019.