A MULTI-INPUT SINGLE OUTPUT (MISO) BUCK CONVERTER DESIGN BY SWITCHED-CAPACITOR (SC) TECHNIQUES

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ABSTRACT. *This paper presents a multi-input single output (MISO) buck converter designed by switched-capacitor (SC) techniques. Unlike existing MISO buck converters, the proposed converter is realized by combining a traditional buck converter and an SC converter with symmetrical structure. The symmetrical SC buck topology of the proposed converter provides higher step-down conversion ratios than existing MISO buck converters. The characteristics of the proposed MISO buck converter are clarified by simulation program with integrated circuit emphasis (SPICE) simulations and breadboard experiments. In the performed simulations, the power efficiency of the proposed MISO converter with two inputs reached more than 95% at 2 Watt. Furthermore, the feasibility of the proposed topology is confirmed in the performed experiments, where the voltage gain was 0.244, 0.195, and 0.148 when the duty factor D was 0.5, 0.4, and 0.3, respectively.*
Keywords: Multi-input single output converters, Buck converters, Step-down converters, Switched-capacitor techniques, Symmetrical topologies

1. **Introduction.** Recently, due to the high demand for the use of renewable energy sources, a multi-input single output (MISO) power converter [1-15] has received many researchers' attention. Distinguished from a traditional single-input single-output (SISO) converter [16-19], the MISO power converter can integrate some energy sources with smaller component count, smaller system size, and lower cost. Depending on the converter topology, the MISO power converters can be divided into inductor-less MISO converters [1-3] and inductor-based MISO converters [4-15]. In particular, the inductor-based MISO topology is commonly apopted for the use of renewable energy sources, because the inductor-less MISO converter suffers from poor output regulation. The inductor-based MISO DC/DC converters can be classified into three types, viz. buck type [4-7], boost type [8-11], and buck-boost type [12-15]. Among others, the MISO buck converter has been employed to convert high voltage renewable energy sources such as photovoltaics (PVs). However, due to the limitation of the duty factor D, existing MISO buck converters utilizing a buck converter [4-6] have small voltage gains. In this paper, we propose a MISO buck converter designed by SC techniques [20]. Unlike existing MISO buck converters [4-7], the proposed converter is realized by combining a traditional buck converter [4-6] and an SC converter with symmetrical structure [21]. In other words, the proposed converter has a hybrid topology [22]. The symmetrical SC buck topology of the proposed

converter provides higher step-down conversion ratios than existing MISO buck converters. The characteristics of the proposed MISO buck converter are clarified by SPICE simulations and breadboard experiments.

This paper is organized as follows. First, Section 1 is the introduction part. Next, Section 2 details the circuit configuration and its operation principle of the proposed converters. Then, Section 3 reveals the characteristics of the proposed converter, such as output voltage and power efficiency, by simulation program with integrated circuit emphasis (SPICE) simulations. After that, Section 4 demonstrates the feasibility of the proposed topology by breadboard experiments. Finally, Section 5 briefly summarizes the results of this work.

2. **Proposed MISO Converter.** Figure 1 illustrates the circuit configuration of the proposed MISO buck converter. The proposed MISO converter is designed by combining the buck converter and the SC converter with symmetrical structure. In the proposed converter, the switches $S_{1,j}$ $(j = 1, \ldots, N)$, S_2, S_3, and S_4 are driven by the clock pulses shown in Figure 2. In this figure, the duty factor D is expressed by T_1/T. To help readers' understanding, the operation principle of the proposed converter is explained concerning the instantaneous equivalent circuits of the simplest proposed MISO converter shown in Figure 3. First, in state-1, the input voltage $V_{in.1,1}$ is divided into $V_{in.1,1}/2$ by the capacitors C_1 and C_2, where $V_{in.1,1}/2$ is provided to the inductor L_1. At the same time, the inductor L_2 is connected to the ground via the switch S_4. Next, in state-2, the electric charges in C_1 and C_2 are averaged S_2 and S_4. Then, in state-3, the input voltage $V_{in.2,1}$
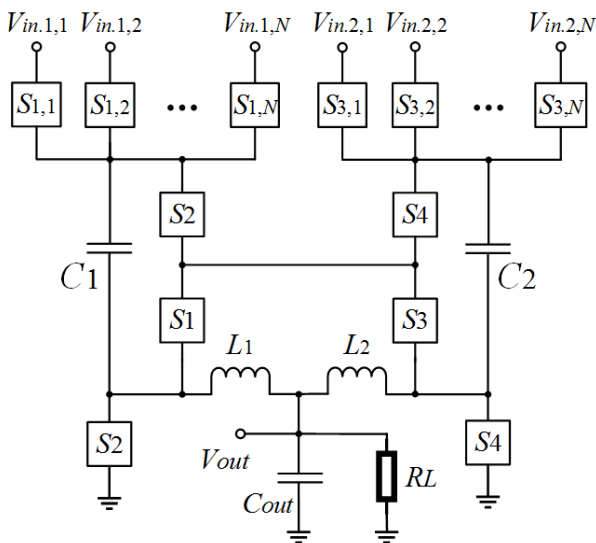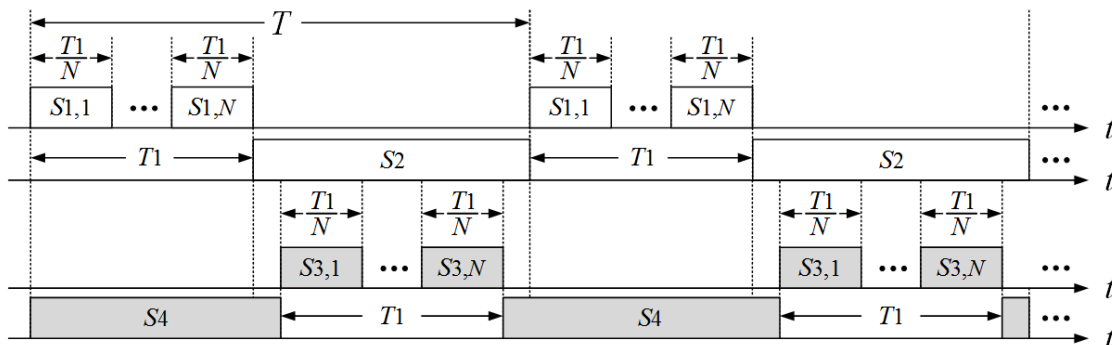

FIGURE 1. Proposed MISO buck converter

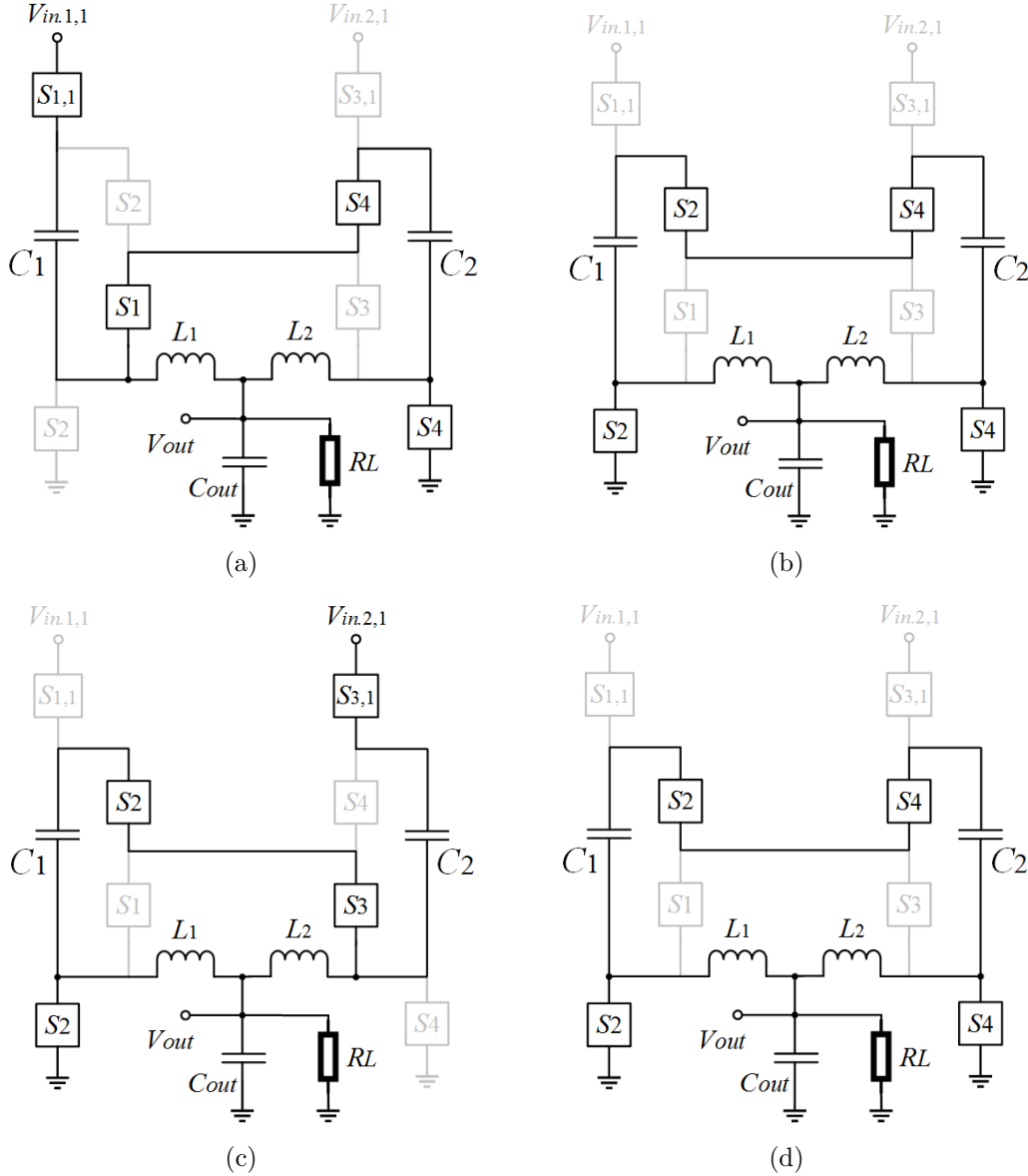FIGURE 2. Operation principle of the proposed MISO buck converter

FIGURE 3. Instantaneous equivalent circuits: (a) state-1, (b) state-2, (c) state-3 and (d) state-4

is divided into $V_{in.2,1}/2$ by the capacitors C_1 and C_2, where $V_{in.2,1}/2$ is provided to the inductor L_2. At the same time, the inductor L_1 is connected to the ground via the switch S_2. Lastly, state-4 has the same process as state-2. By repeating these four-processes, the output voltage V_{out} is provided to the output load R_L, because L_1 and L_2 are driven by the clock pulses with an amplitude of $V_{in.1,1}/2 \ (= V_{in.2,1}/2)$.

Next, we analyze the characteristics of the proposed converter shown in Figure 3, where we assumed that $i)$ time constant is much larger than T and $ii)$ parasitic elements are almost negligible. In a steady-state condition, the variation of electric charges satisfies the following conditions:

$$
\begin{aligned}
\text{State-1:} \qquad & \Delta q_{T_1,v_{in1,1}} = \Delta q_{T_1}^{C_1}, \quad \Delta q_{T_1,v_{in2,1}} = 0, \\
& \Delta q_{T_1,v_{out}} = \Delta q_{T_1}^{L_1} + \Delta q_{T_1}^{L_2} - \Delta q_{T_1}^{out}, \\
& \text{and } \Delta q_{T_1}^{C_1} = \Delta q_{T_1}^{C_2} + \Delta q_{T_1}^{L_1}. \\
\text{State-2:} \qquad & \Delta q_{T_2,v_{in1,1}} = \Delta q_{T_2,v_{in2,1}} = 0, \\
& \Delta q_{T_2,v_{out}} = \Delta q_{T_2}^{L_1} + \Delta q_{T_2}^{L_2} - \Delta q_{T_2}^{out},
\end{aligned}
\tag{1}
$$

$$\text{and } \Delta q_{T_2}^{C_1} + \Delta q_{T_2}^{C_2} = 0. \tag{2}$$

$$\text{State-3:} \qquad \Delta q_{T_3, v_{in1,1}} = 0, \quad \Delta q_{T_3, v_{in2,1}} = \Delta q_{T_3}^{C_2},$$

$$\Delta q_{T_3, v_{out}} = \Delta q_{T_3}^{L_1} + \Delta q_{T_3}^{L_2} - \Delta q_{T_3}^{out},$$

$$\text{and } \Delta q_{T_3}^{C_2} = \Delta q_{T_3}^{C_1} + \Delta q_{T_3}^{L_2}. \tag{3}$$

$$\text{State-4:} \qquad \Delta q_{T_4, v_{in1,1}} = \Delta q_{T_4, v_{in2,1}} = 0,$$

$$\Delta q_{T_4, v_{out}} = \Delta q_{T_4}^{L_1} + \Delta q_{T_4}^{L_2} - \Delta q_{T_4}^{out},$$

$$\text{and } \Delta q_{T_4}^{C_1} + \Delta q_{T_4}^{C_2} = 0. \tag{4}$$

In (1)-(4), $\Delta q_{T_k, v_{in1,1}}$ $(k = 1, 2, 3, 4)$ is the variation of electric charge in $V_{in1,1}$, $\Delta q_{T_k, v_{in2,1}}$ is the variation of electric charge in $V_{in2,1}$, $\Delta q_{T_k}^{C_i}$ $(i = 1, 2)$ is the variation of electric charge in the capacitor C_i, $\Delta q_{T_k}^{L_i}$ $(i = 1, 2)$ is the variation of electric charge in the inductor L_i, and $\Delta q_{T_k, v_{out}}$ is the variation of electric charge in V_{out}, where the overall change in the electric charges, $\Delta q_{T_i}^{C_i}$, is zero. Using (1)-(4), the I/O currents of the proposed MISO converter can be obtained as

$$I_{in1,1} = \sum_{k=1}^{4} \Delta q_{T_k, v_{in1,1}}/T = \Delta q_{T_1}^{C_1}/T, \tag{5}$$

$$I_{in2,1} = \sum_{k=1}^{4} \Delta q_{T_k, v_{in2,1}}/T = \Delta q_{T_3}^{C_2}/T, \tag{6}$$

$$\text{and } I_{out} = \sum_{k=1}^{4} \Delta q_{T_k, v_{out}}/T = I_L, \tag{7}$$

if L_1 and L_2 are operated in a continuous-mode. In (7), I_L is the maximum inductor current in a steady state. Since the proposed MISO converter has a symmetrical topology, the input currents satisfy

$$I_{in1,1} = I_{in2,1}. \tag{8}$$

Substituting (1)-(4) and (8) into (5)-(7), we have

$$I_{out} = \frac{2}{D}(I_{in1,1} + I_{in2,1}), \tag{9}$$

where D is a duty factor of clock pulses, T_1/T. From (8), the relationship between the I/O voltages can be expressed as

$$V_{out} = \frac{D}{2}(V_{in1,1} + V_{in2,1}) \tag{10}$$

because we assumed that parasitic elements are almost negligible in this analysis. It can be seen from (10), the voltage gain of the proposed MISO buck converter is $D/2$. On the other hand, the gain of the conventional MISO buck converter [4-6] is D. Therefore, the proposed MISO converter can achieve higher step-down conversion ratio than the conventional MISO buck converter.

3. **Simulation.** Concerning the proposed MISO converter with 2 inputs, we performed SPICE simulations under the conditions that $V_{in1,1} = V_{in2,1} = 15$ V, $R_{on} = 0.1$ Ω, $T = 10$ μs, $C_1 = C_2 = 33$ μF, $C_{out} = 100$ μF, and $L_1 = L_2 = 10$ μH. The simulated results are shown in Figure 4, where Figure 4(a) illustrates the output voltage as a function of output power and Figure 4(b) describes the power efficiency as a function of output power. Since the voltage gain of the proposed MISO converter is $D/2$, the ideal voltage gain is 0.25, 0.2, and 0.15 when the duty factor D is 0.5, 0.4, and 0.3, respectively. From Figure 4(a), the simulated gain of the proposed MISO converter is 0.247, 0.196, and 0.149 at 2 Watt when D is 0.5, 0.4, and 0.3, respectively. From Figure 4(b), the power efficiency of the
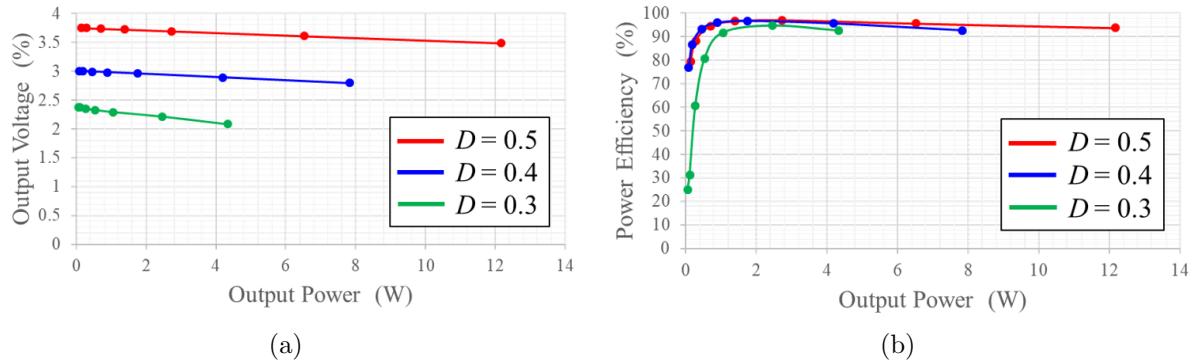
FIGURE 4. Simulated result: (a) output voltage and (b) power efficiency

proposed MISO converter reaches about 96%, 96%, and 95% at 2 Watt when D is 0.5, 0.4, and 0.3, respectively.

4. **Experiment.** To perform simple topology confirmation, some breadboard experiments were conducted regarding the proposed converter with 2 inputs, where $V_{in1,1} =$

TABLE 1. Circuit components

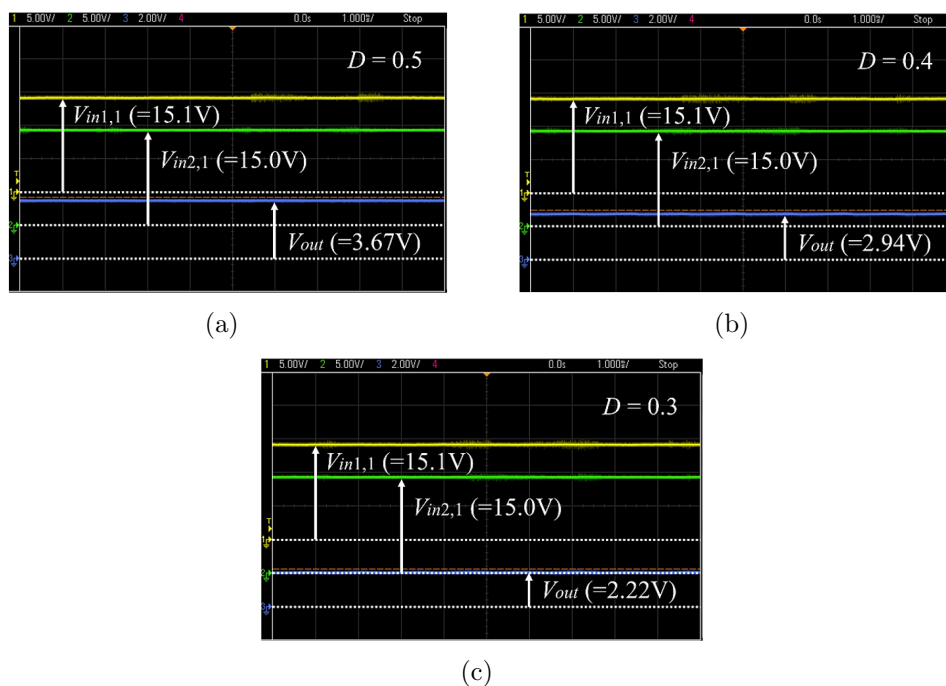| Parts	Components	Models
Main block	Switch	AQV212
	Capacitors C_1 and C_2	33 μF
	Capacitor C_{out}	200 μF
	Inductors L_1 and L_2	30 mH
Control block	Micro controller	PIC12F629-I/P
	Darlington driver IC	TD6203APG
	Current control resistance	330 Ω
Output load	Resistance	2 kΩ

FIGURE 5. Measured output voltage: (a) $D = 0.5$, (b) $D = 0.4$ and (c) $D = 0.3$

$V_{in2,1} = 15$ V, $T = 2.5$ ms, $C_1 = C_2 = 33$ µF, $C_{out} = 200$ µF, and $L_1 = L_2 = 30$ mH. In the performed experiments, the experimental circuit was built with the circuit components shown in Table 1, where the switching frequency f was set to 400 Hz due to slow switching speed of the photo MOS relays AQV212. Figure 5 demonstrates the measured output voltage of the experimental circuit. As it can be seen from Figure 5, the voltage gain of the proposed MISO converter is 0.244 (= 3.67 V/15.05 V), 0.195 (= 2.94 V/15.05 V), and 0.148 (= 2.22 V/15.05 V) when the duty factor D is 0.5, 0.4, and 0.3, respectively. From the obtained results, the feasibility of the proposed topology can be confirmed.

5. **Conclusions.** In this paper, we proposed MISO buck converter designed by using SC techniques. Owing to the symmetrical SC buck topology, the proposed MISO converter can provide a high step-down conversion ratio. In the performed computer simulations, the power efficiency of the proposed MISO converter with two inputs reached more than 95% at 2 Watt. Furthermore, the feasibility of the proposed topology was confirmed by breadboard experiments, where the voltage gain was 0.244, 0.195, and 0.148 when the duty factor was 0.5, 0.4, and 0.3, respectively. However, only the feasibility of the proposed topology was confirmed in the experiments, because we conducted the breadboard experimental tests. In a future study, the proposed MISO back converter will be assembled on a printed wiring board for detailed evaluation.

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