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PROPOSAL OF 2-INPUT SHL CIRCUIT WITH FG CALIBRATION

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Abstract. *A 2-input Soft-Hardware-Logic circuit (SHL circuit) behaves 16 logic functions for 2 input signals by changing three control signals. However, the 2-input SHL circuit has a floating gate in a νCMOS inverter. The effect of the initial charge on the floating gate causes the neuron MOS circuit to behave unexpectedly. In this paper, we propose a new 2-input SHL circuit with FG calibration to be stable, and show that the proposed circuit satisfies the same logical functions as the conventional SHL circuit by HSPICE simulation.*

Keywords: Neuron MOS transistor, Neuron CMOS inverter, SHL circuit, Floating gate, FG calibration

1. **Introduction.** A neuron MOS transistor (νMOS) calculates the weighted sum of multiple input voltages and performs the threshold operation based on the weighted sum [1].

The 2-input Soft-Hardware-Logic circuit (SHL circuit) was realized by a neuron CMOS inverter (νCMOS) using the νMOS. The feature of the 2-input SHL circuit is that 16 kinds of logical functions are realized for 2 input signals by changing 3 control signals. However, νCMOS has a floating gate (FG) that is not connected anywhere of the circuit and FG is affected by the initial charge and causes malfunction [2-5]. In the conventional 2-input SHL circuit, this problem was canceled to zero by UV (ultraviolet light) irradiation technique, which is well known for EPROM erasing [6]. However, this task takes a very long time.

We use the FG calibration (FGC) circuit, which connects the FG and the output of νCMOS through an nMOS switch and nullifies the effect of the charge accumulated in the FG [7,8].

In this paper, we introduce FGC to the 2-input SHL circuit. We propose a 2-input SHL circuit with FGC and show that the proposed circuit satisfies the same logic functions as the conventional 2-input SHL circuit by HSPICE simulation. And we show that the problem of FG is solved by FGC circuit.

This paper consists of 5 chapters. First, Chapter 1 is an introduction and describes the research background, research purpose, and structure of this paper. Next, Chapter 2 describes the circuit configuration of the conventional 2-input SHL circuit and the problems of the conventional 2-input SHL circuit. Chapter 3 describes the circuit configuration of the proposed circuit and the solution to the problem of initial charge by the FGC circuit. Chapter 4 considers the simulation conditions and simulation result. Finally, Chapter 5 is a conclusion and summarizes the results obtained in this study. Furthermore, the remaining issues are described.

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2. Conventional 2-Input SHL Circuit.

2.1. **Circuit configuration.** The 2-input SHL circuit is given in Figure 1. The 2-input SHL circuit consists of a 2-bit D/A converter, three pre-νCMOS ($\nu\mathrm{CMOS_{PA}}$, $\nu\mathrm{CMOS_{PB}}$, $\nu\mathrm{CMOS_{PC}}$), and a main-νCMOS ($\nu\mathrm{CMOS_M}$). $\mathrm{FG_A}$, $\mathrm{FG_B}$, and $\mathrm{FG_C}$ are the floating gates of $\nu\mathrm{CMOS_{PA}}$, $\nu\mathrm{CMOS_{PB}}$, and $\nu\mathrm{CMOS_{PC}}$ respectively, and $\mathrm{FG_M}$ is the floating gate of $\nu\mathrm{CMOS_M}$. X_1 and X_2 are input signals ("0" or "1"). V_A, V_B, and V_C are the control signals and may use $V_{DD}/4$, $V_{DD}/2$ and $3V_{DD}/4$ in addition to "0" and V_{DD}. It is assumed that the binary number "0" is associated with 0 [V] and "1" is associated with V_{DD} [V]. And V_{OUT} is the output voltage. By supplying an appropriate voltage to V_A, V_B, and V_C 16 kinds of logical functions are expressed.

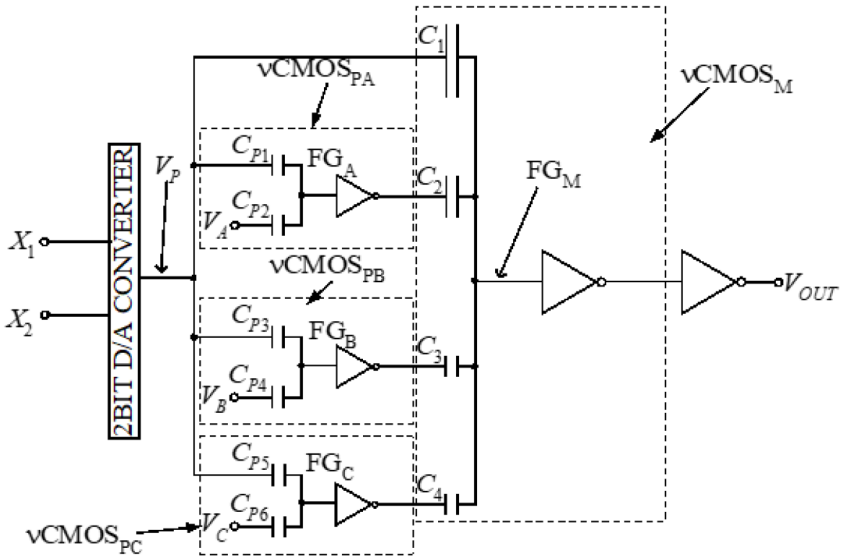

FIGURE 1. Conventional 2-input SHL circuit

2.2. **Circuit problem.** The 2-input SHL circuit may do not work due to the influence of the electric charge accumulated in the FG. The simulation affected by the initial charge is shown in Chapter 4. The 2-input SHL circuit has not been able to solve the FG problem in the circuit. The 2-input SHL circuit uses a UV erasing technique. The UV erasing technique is a method to solve the problem of FG by irradiating the upper part of the chip with the UV after making the chip. However, this way takes a very long time to irradiate the UV and solve the FG problem. Therefore, we propose a circuit that solves the problem of FG in the circuit.

3. Proposed Circuit.

3.1. **Circuit configuration.** We propose a new circuit whose name is a 2-input SHL circuit with FG calibration. FGC connects the FG and the output of νCMOS through an nMOS switch and nullifies the effect of the charge accumulated in the FG. A simple example illustrating the new scheme is given in Figure 2. This circuit behaves 16 logic functions for 2 input signals by changing 3 control signals. The proposed circuit consists of the 2-bit D/A converter, three pre-νCMOS ($\nu\mathrm{CMOS_{PA}}$, $\nu\mathrm{CMOS_{PB}}$, $\nu\mathrm{CMOS_{PC}}$), and a main νCMOS ($\nu\mathrm{CMOS_M}$). $\mathrm{FG_A}$, $\mathrm{FG_B}$, and $\mathrm{FG_C}$ are floating gates of $\nu\mathrm{CMOS_{PA}}$, $\nu\mathrm{CMOS_{PB}}$, and $\nu\mathrm{CMOS_{PC}}$ and $\mathrm{FG_M}$ is a floating gate of $\nu\mathrm{CMOS_M}$. C_{P1} and C_{P2} are the gate capacitances of $\nu\mathrm{CMOS_{PA}}$ and are designed to be $C_{P1} : C_{P2} = 1 : 1$. C_{P3} and C_{P4} are the gate capacitances of $\nu\mathrm{CMOS_{PB}}$ and are designed to be $C_{P3} : C_{P4} = 1 : 1$. C_{P5} and C_{P6} are the gate capacitances of $\nu\mathrm{CMOS_{PC}}$ and are designed to be $C_{P5} : C_{P6} = 1 : 1$. C_{M1}, C_{M2}, C_{M3}, and C_{M4} are the gate capacitances of $\nu\mathrm{CMOS_M}$, and designed to be

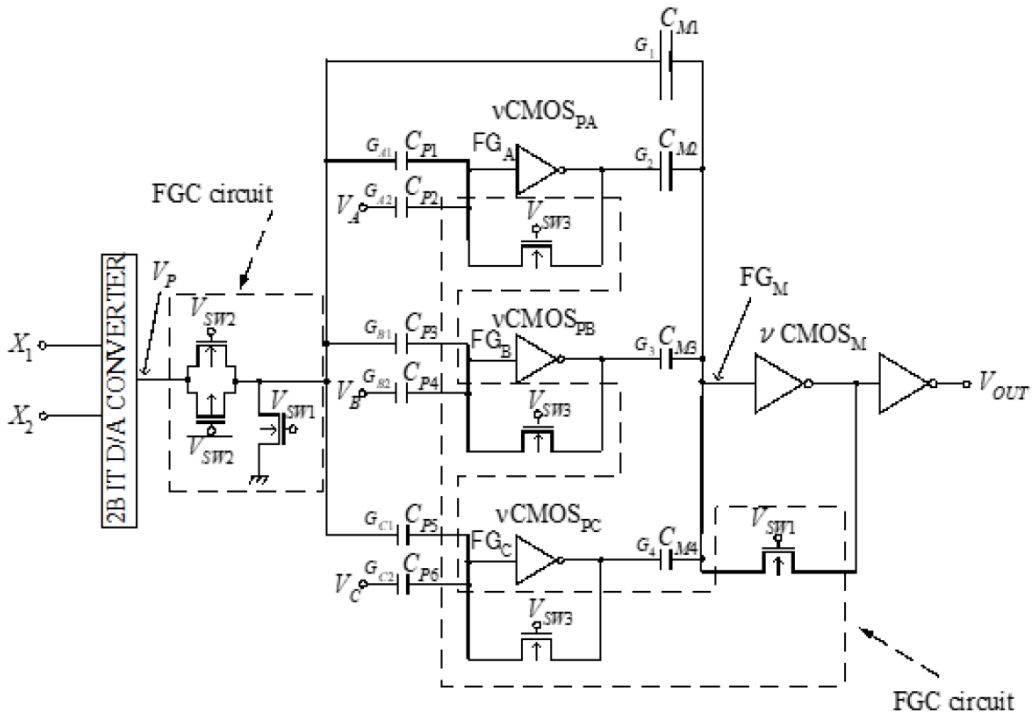

FIGURE 2. SHL circuit with FG calibration

$C_{M1} : C_{M2} : C_{M3} : C_{M4} = 4 : 2 : 1 : 1$. X_1 and X_2 are the input signals ("0" or "1"), and V_A, V_B, and V_C are the control signals and may use $V_{DD}/4$, $V_{DD}/2$ and $3V_{DD}/4$ in addition to "0" and V_{DD}. It is assumed that the binary number "0" is associated with 0 [V] and "1" is associated with V_{DD} [V]. And V_{OUT} is the output voltage. The V_P is connected to the 2-bit D/A converter via a CMOS switch from the input signals X_1 and X_2. If you enter the voltage $(X_1, X_2) = (0, 0)$, $(1, 0)$, $(0, 1)$, $(1, 1)$, it is designed to generate an analog voltage $V_P = V_{DD}/8$, $3V_{DD}/8$, $5V_{DD}/8$, $7V_{DD}/8$.

The circuit configuration described above is the same as the conventional 2-input SHL circuit shown in Figure 1. However, the proposed circuit can solve the problem of FG in the circuit. V_{SW1}, V_{SW2}, and V_{SW3} are the switches for performing FGC operation, and the inversion threshold voltage V_{INV} of each νCMOS is designed to be $V_{DD}/2$.

3.2. **FGC operation of the circuit.** The 2-input SHL circuit with FGC operates in three phases. During Phase 1, V_{DD} is applied to V_A, V_B, and V_C. Then, by setting V_{SW1} to "1", V_{SW2} to "0", and V_{SW3} to "1", the voltage of each FG is set to $V_{DD}/2$ regardless of the charge of each FG by short-circuiting the output terminal of each νCMOS and each FG.

During Phase 2, V_{SW3} of νCMOS$_{PA}$, νCMOS$_{PB}$, νCMOS$_{PC}$ are set to "0" and the voltages of V_A, V_B, and V_C are set to "0". As a result, the output terminal of νCMOS$_{PA}$, νCMOS$_{PB}$, νCMOS$_{PC}$ and FG$_A$, FG$_B$, FG$_C$ are separated, and the voltages of FG$_A$, FG$_B$, FG$_C$ become "0".

During Phase 3, the output terminals of νCMOS$_M$ and FG$_M$ are separated by setting V_{SW1} to "1".

After the end of all phases, set V_{SW2} to "0" and start the logical operation. Then V_A, V_B, and V_C are supplied the voltage (0, $V_{DD}/4$, $V_{DD}/2$, $3V_{DD}/4$, V_{DD}) shown in Table 1, and the 2-input SHL circuit with FGC behaves 16 logic functions as shown in V_{OUT} in Table 1. The result of the simulation is shown in Chapter 4.

TABLE 1. Control signal and output voltage

V_A	V_B	V_C	V_{OUT}	V_A	V_B	V_C	V_{OUT}
V_{DD}	V_{DD}	V_{DD}	0	$3V_{DD}/4$	$3V_{DD}/4$	$3V_{DD}/4$	NOR
V_{DD}	V_{DD}	0	AND	$3V_{DD}/4$	$3V_{DD}/4$	0	XNOR
$V_{DD}/4$	V_{DD}	V_{DD}	$\overline{X_1} \cdot X_2$	$V_{DD}/4$	$3V_{DD}/4$	$3V_{DD}/4$	X_1
V_{DD}	0	0	X_1	$3V_{DD}/4$	0	0	$\overline{X_1} + X_2$
$V_{DD}/2$	$V_{DD}/2$	V_{DD}	$X_1 \cdot \overline{X_2}$	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	$\overline{X_2}$
$V_{DD}/2$	V_{DD}	0	X_2	$V_{DD}/2$	$V_{DD}/2$	0	$X_1 + \overline{X_2}$
$V_{DD}/4$	$V_{DD}/4$	V_{DD}	XOR	$V_{DD}/4$	$V_{DD}/4$	$V_{DD}/4$	NAND
0	0	V_{DD}	OR	0	0	0	1

TABLE 2. Device parameters and simulation conditions

Symbol	Description	Value	Units
V_{DD}	Power supply voltage	1.8	V
GND	Ground voltage	0	V
W_n/L_n	Width/Length of nMOS	1.0/0.18	μm
W_p/L_p	Width/Length of pMOS	3.0/0.18	μm
C_{Pi}, $(i = 1, 2, 3, 4, 5, 6)$	Capacitance	16	fF
C_{Mi}, $(i = 1, 2, 3, 4)$	Capacitance	16	fF

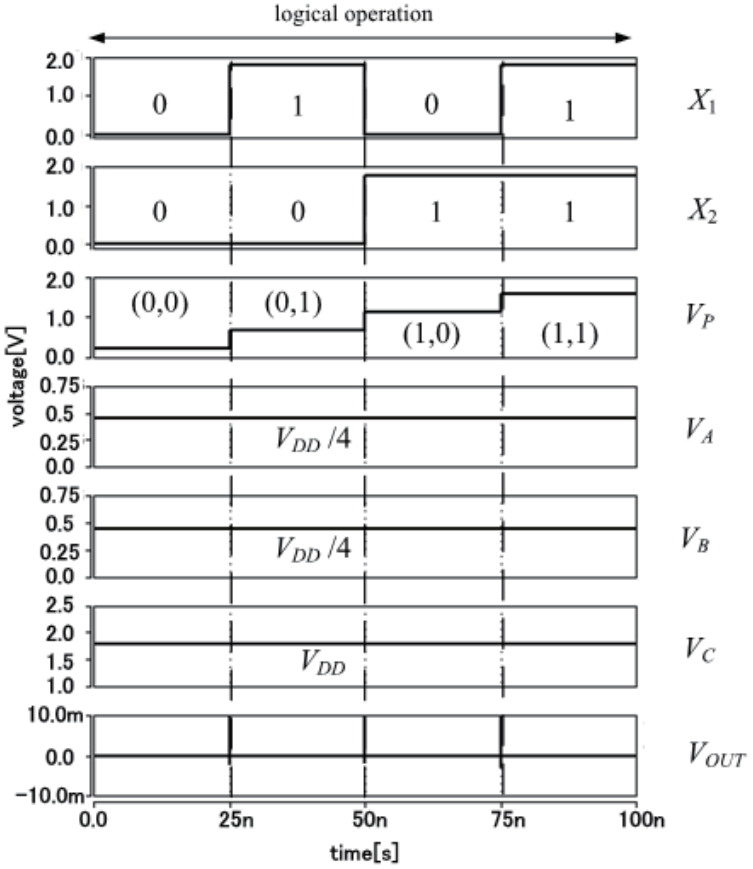

FIGURE 3. Simulation of the 2-input SHL circuit

4. **Control Design.** The proposed circuit was HSPICE simulated with the device parameters in Table 2. The simulation of the conventional 2-input SHL circuit is shown in Figure 3.

The simulation of the new 2-input SHL circuit with FGC is shown in Figure 4.

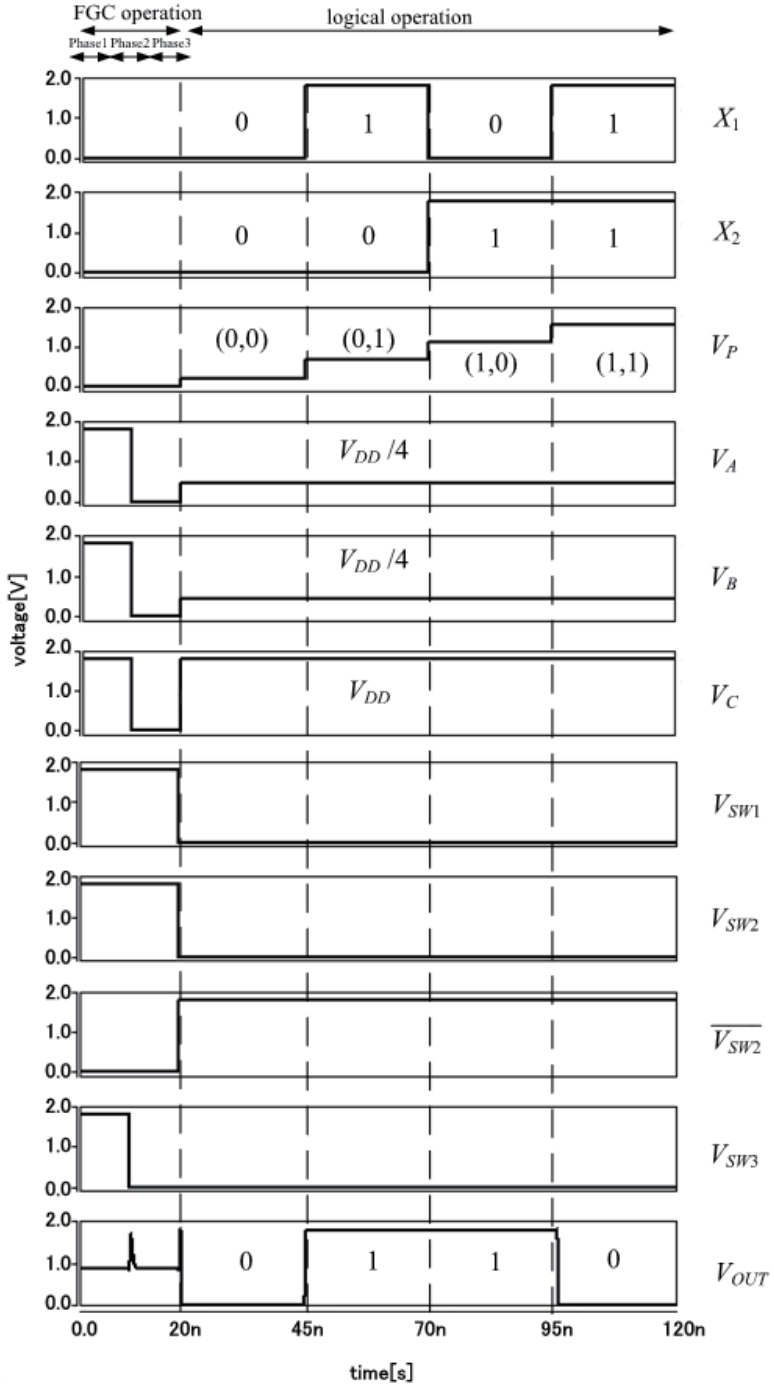

FIGURE 4. Simulation of the 2-input SHL circuit with FG calibration

By setting the input signals X_1 and X_2 to $(0,0)$, $(1,0)$, $(0,1)$, $(1,1)$, the output signal V_P becomes $V_{DD}/8$, $3V_{DD}/8$, $5V_{DD}/8$, $7V_{DD}/8$. It is confirmed that this is the same movement as described in Chapter 3. In Figure 3, we try to express EXOR by setting $V_A = V_{DD}/4$, $V_B = V_{DD}/4$, and $V_C = V_{DD}$. However, this simulation does not express EXOR. From this result, it is shown that the FG of **ν**CMOS is affected by the initial charge and causes malfunction.

In Figure 4, we have succeeded in expressing EXOR by setting $V_A = V_{DD}/4$, $V_B = V_{DD}/4$, and $V_C = V_{DD}$. From this result, it can be seen that the FGC circuit operates normally. And the influence of the initial charge is nullified. Moreover, in this simulation, the movements from Phase 1 to Phase 3 of FGC operation are performed between 0.0 and 20n (s). Also, it was confirmed that 16 kinds of logical functions are expressed by

simulating as shown in Table 1. The 2-input SHL circuit with FGC causes more temporal loss than the conventional 2-input SHL circuit. The reason for this is that by incorporating the FGC circuit, it takes time to negate the influence of the initial charge accumulated in the FG. However, the loss of this time has solved the problem of FG, which could not be solved by the conventional 2-input SHL circuit.

5. **Conclusions.** We proposed the new 2-input SHL circuit with FG calibration. We also simulated the circuit and confirmed that the proposed circuit behaves 16 logical functions for 2 input signals by changing 3 control signals. It was confirmed that the problem of FG was solved by introducing the FGC circuit. The new 2-input SHL circuit with FG calibration causes more temporal loss than the conventional 2-input SHL circuit to solve the problem of FG.

In the future, this circuit will be converted into a chip and tested on an actual machine. This confirms whether the effect of the initial charge, which is the ultimate goal of this study, can be really nullified.

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