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THE EXPERIMENT OF K^N VOLTAGE GAIN SWITCHED-CAPACITOR DC-DC CONVERTER BASED ON PARALLEL FIBONACCI-TYPE CONVERTER

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Abstract. *Environmental pollution has a great impact on the earth due to demand energy. Therefore, clean energy harvesting systems are one of the key technologies to solve the environmental pollution problem. Together with the development of clean energy harvesting and energy conversion into electrical energy, another important area of research will be the development of high-efficiency converters. This paper proposes one form of switched-capacitor (SC) DC-DC converters that can be improved to become a chip at the smallest possible size, viz. a Fibonacci parallel-connected SC DC-DC converter for energy harvesting system. The proposed converter can realize high voltage gain with* $K^N \times V_{in}$, *(*$N, K = 1, 2, 3, \ldots$*), and minimize the occupational chip area by untroubled from the ripple noise problem, because a stepped-up voltage charges an output capacitor every clock cycle. Unlike traditional converters, the ripple noise of the proposed converter becomes quite small. Therefore, the proposed converter is appropriate for energy harvesting systems utilizing uncommon energy sources. The assessment of the proposed converter is rendered by theoretical analysis and experiments.*

Keywords: Charge pump, Cross-connected topology, Energy harvesting system, Fibonacci converters

1. **Introduction.** Clean energy harvesting [1-5] is one of the most promising technologies to solve the environmental pollution problem. In energy harvesting systems, ambient energy is collected by energy harvesting devices and is converted by power converters. Therefore, in the development of efficient energy harvesting systems, the design of the high-efficiency converters is a key issue. A widespread converter is the inductor converter, which can achieve high efficiency. However, it suffers from electromagnetic interference (EMI) and large volume of magnetic components. This paper proposes one form of switched-capacitor (SC) DC-DC converters [6-8] that can be improved to become a chip at the smallest possible size. The size and signal of energy harvesting systems utilizing uncommon energy sources, such as force, and vibration, are normally small. Therefore, the converter should have a high voltage gain [9,10]. In around this decade, a lot of SC DC-DC converters have been continuously studied. For example, several types of charge pump converters were proposed by Wang et al. [11] and Yun et al. [12,13]. The voltage gain of the charge pump converter is expressed as $N \times V_{in}$ ($N = 1, 2, 3, \ldots$), where N is the number of stages and V_{in} is a DC input. However, the voltage gain of the charge pump converter is small. Therefore, the charge pump converter requires many circuit components to achieve a high voltage gain, because the energy harvesting device provides a small voltage. The Fibonacci SC DC-DC converter was suggested by Eguchi et al. [14-17]. The voltage gain of the Fibonacci converter can provide high voltage with last state plus second-last state, viz. $V_{N-1} + V_{N-2}$ ($N = 1, 2, 3, \ldots$). The drawback of the

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Fibonacci converter is a large occupational chip area. The Fibonacci converter requires a large output capacitor to reduce output ripple, because a stepped-up voltage charges an output capacitor a half clock cycle. The SC DC-DC converter with SCVM (switched capacitor voltage multiplier) topology is designed by Chang and Kuo [18-20]. By connecting series-parallel type SC converter cells in series, the SCVM converter can provide a high voltage, viz. $N \times M \times V_{in}$ $(N, M = 1, 2, 3, \ldots)$. However, the SCVM suffers from low power efficiency, because some series-parallel type SC converter cells are connected in series to achieve high gain. The cross-connected charge pump [21,22] was suggested by Eguchi et al., where the voltage gain of the converter is $2N \times V_{in}$ $(N = 1, 2, 3, \ldots)$. The cross-connected charge pump can minimize the size of the output capacitor, because the electric charge of an output capacitor is provided to an output load in all clock cycles. However, the circuit size becomes large by connecting many stages to make high voltages gain when input voltages are small.

In this paper, we present a Fibonacci parallel connected SC DC-DC converter for energy harvesting systems. The proposed converter can realize high voltage gain with $K^N \times V_{in}$ $(N, K = 1, 2, 3, \ldots)$, and minimize the occupational chip area by untroubled from the ripple noise problem, because a stepped-up electric generated in the output capacitor is charged every clock cycle. Unlike traditional converters, the ripple noise of the proposed converter becomes quite small. Therefore, the proposed converter is suitable for energy harvesting systems. The performance of the proposed converter is clarified by theoretical analysis and experiments.

The rest of this paper is organized as follows. First, the topology of the proposed converter and its operation principle are described in Section 2. Next, the characteristics of the proposed converter are analyzed theoretically in Section 3, where the theoretical formulas for calculating the maximum power efficiency and output voltage are derived by using a four-terminal equivalent model [23,24]. Then, to confirm the feasibility of the proposed topology, some experiments are conducted in Section 4. Finally, the result and future study of this work are briefly summarized in Section 5.

2. Circuit Configuration.

2.1. Traditional converter.

Figure 1 illustrates the circuit configuration of the traditional Fibonacci converter with N stages, where the switches S_1 and S_2 are controlled by the two-phase clock pulses Φ_1 and Φ_2. The output voltage of the traditional Fibonacci converter is expressed as

$$V_{out} = V_{N-1} + V_{N-2} \quad (N \geq 0), \tag{1}$$

where the parameter N is an integer number that shows the number of stages of the traditional Fibonacci converter. Substituting N with $(N = 1, 2, 3, 4)$ into (1), the output voltage of the traditional Fibonacci converter becomes

$$\begin{aligned} V_{out} &= V_{in} + V_{in} = 2V_{in}, \quad (N = 1), \\ V_{out} &= V_{in} + 2V_{in} = 3V_{in}, \quad (N = 2), \\ V_{out} &= 2V_{in} + 3V_{in} = 5V_{in}, \quad (N = 3), \\ \text{and } V_{out} &= 3V_{in} + 5V_{in} = 8V_{in}, \quad (N = 4). \end{aligned} \tag{2}$$

In the traditional Fibonacci converter, the stepped-up voltage V_{out} charges the output capacitor C_{out} a half clock cycle. Therefore, to reduce output ripple, a large output capacitor is required.

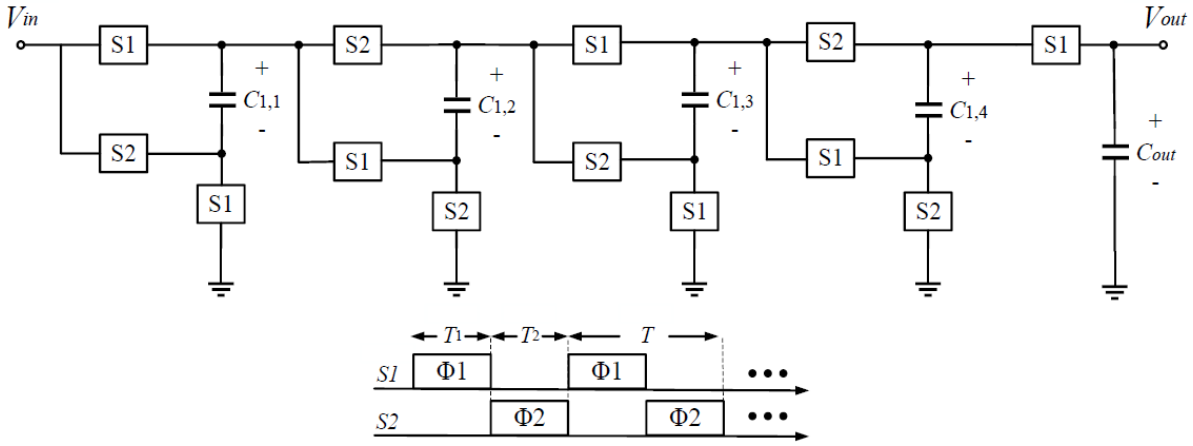

FIGURE 1. Circuit configuration of the 4-stage traditional Fibonacci converter

2.2. **Proposed converter.** Figure 2 depicts the block diagram of the proposed converter with N stages, where the switches $S_1, \ldots, S_K$ are controlled by the K-phase clock pulses. The output voltage of the traditional Fibonacci converter is equal to

$$V_{out} = K^N \times V_{in} \quad (N, K \geq 0). \tag{3}$$

As (3) shows, the proposed converter can provide higher voltage gain than the traditional Fibonacci converter. Unlike the traditional Fibonacci converter, the stepped-up voltage V_{out} charges the output capacitor C_{out} every clock cycle. Therefore, the circuit size of the proposed converter is smaller than that of the traditional Fibonacci converter, because a big output capacitor is not required. For this reason, the proposed converter is reasonable to become a chip for energy harvesting systems utilizing an uncommon source.

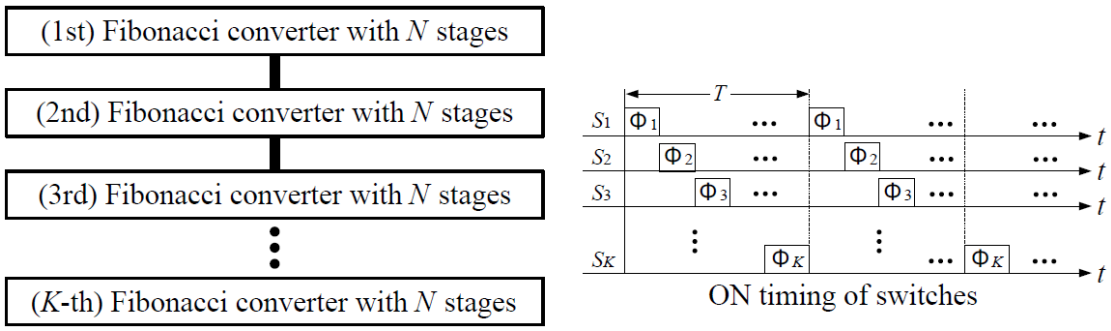

FIGURE 2. Block diagram of the proposed converter with N stages

3. **Theoretical Analysis and Comparison.** The total energy consumption of the proposed converter is analyzed theoretically by using the four-terminal equivalent model [23,24] shown in Figure 3. In this figure, the total energy consumption can be calculated by

$$W_T = R_{sc}(\Delta q_{V_{out}})^2/T. \tag{4}$$

In the proposed converter, the instantaneous equivalent circuits are expressed by Figure 4, where R_{on} is the on-resistance of the switch. In these figures, the differential value of electric charges $\Delta q_{T_i}^{i,j}$ of the capacitor $C_{i,j}$ $((i = 1, 2, \ldots, K)$ and $(j = 1, 2, \ldots, N))$ satisfies

$$\Delta q_{T_1}^{i,j} + \Delta q_{T_2}^{i,j} + \cdots + \Delta q_{T_K}^{i,j} = 0, \tag{5}$$

because the sum of the variation of $\Delta q_{T_i}^{i,j}$ is zero. In (5), the period T satisfies

$$T = T_1 + T_2 + \cdots + T_K \text{ and } T/K = T_1 = T_2 = \cdots = T_K. \tag{6}$$

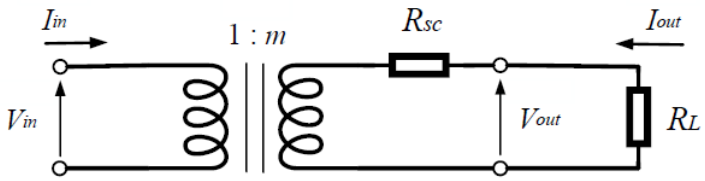

FIGURE 3. Four-terminal equivalent model

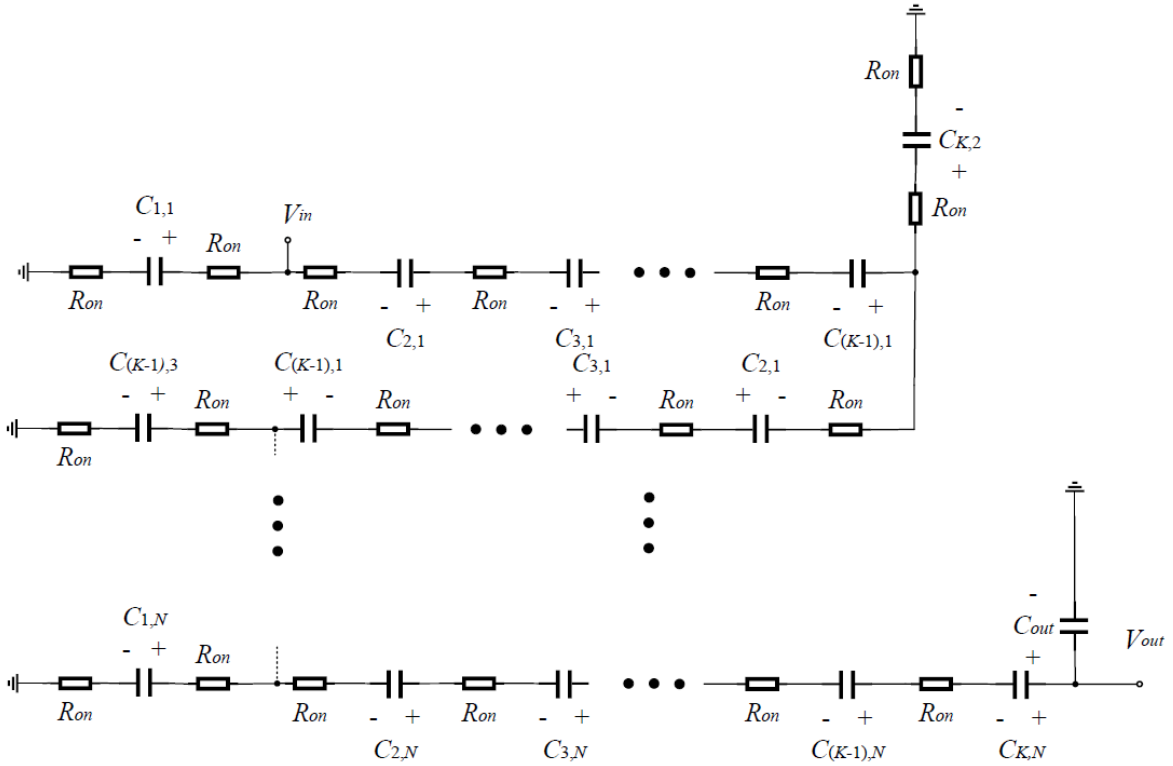

FIGURE 4. Instantaneous equivalent circuits in state-1

Since the proposed converter has symmetrical structure, the topology of all instantaneous equivalent circuits is the same. Therefore, the proposed converter can be analyzed by only the instantaneous equivalent circuits of state-1 (when the switch S_1 is on) shown in Figure 4. Applying the Kirchhoff's Current Law to Figure 4, the differential value of electric charges in state-1 can be expressed as

$$
\begin{aligned}
&\Delta q_{T_1,V_{out}} = \Delta q_{T_1}^{out} + \Delta q_{T_1}^{K,N},\\
&\Delta q_{T_1,V_{in}} = \Delta q_{T_1}^{1,1} - \Delta q_{T_1}^{2,1},\\
&\Delta q_{T_1}^{2,1} = \Delta q_{T_1}^{3,1} = \cdots = \Delta q_{T_1}^{K,1} \neq \Delta q_{T_1}^{1,1},\\
&\Delta q_{T_1}^{1,2} = \Delta q_{T_1}^{K,2} + \Delta q_{T_1}^{K,1},\\
&\Delta q_{T_1}^{1,2} = \Delta q_{T_1}^{2,2} = \cdots = \Delta q_{T_1}^{(K-1),2} \neq \Delta q_{T_1}^{K,2},\\
&\Delta q_{T_1}^{2,3} = \Delta q_{T_1}^{(K-1),3} + \Delta q_{T_1}^{(K-1),2},\\
&\Delta q_{T_1}^{1,3} = \Delta q_{T_1}^{2,3} = \cdots = \Delta q_{T_1}^{(K-3),3} = \Delta q_{T_1}^{(K-2),3} = \Delta q_{T_1}^{K,3} \neq \Delta q_{T_1}^{(K-1),3},\\
&\cdots\\
&\Delta q_{T_1}^{1,N} = \Delta q_{T_1}^{1,(N-1)} + \Delta q_{T_1}^{1,N},\\
&\Delta q_{T_1}^{2,N} = \Delta q_{T_1}^{3,N} = \cdots = \Delta q_{T_1}^{K,N} \neq \Delta q_{T_1}^{1,N}.
\end{aligned}
\tag{7}
$$

Furthermore, the average input and output current, I_{in} and I_{out}, can be expressed as

$$I_{in} = \Delta q_{V_{in}}/T = (\Delta q_{T_1,V_{in}} + \Delta q_{T_2,V_{in}} + \cdots + \Delta q_{T_K,V_{in}})/T$$
$$\text{and} \quad I_{out} = \Delta q_{V_{out}}/T = (\Delta q_{T_1,V_{out}} + \Delta q_{T_2,V_{out}} + \cdots + \Delta q_{T_K,V_{out}})/T. \tag{8}$$

By calculating (6)-(8), the relationship between I_{in} and I_{out} is obtained as

$$I_{in} = -K^N \times I_{out} \text{ and } \Delta q_{V_{in}} = -K^N \times \Delta q_{V_{out}}. \tag{9}$$

Next, the total energy consumption is analyzed for the time period T_1 in order to obtain the total energy consumption equation in terms of (4). From Figure 4, the total consumed energy is obtained as

$$W_T = k^2 \left[\sum_{i=1}^{N} 2R_{on} \left[\frac{(k-1)\Delta q_{V_{out}}}{k^{\{-i+(N-1)\}}} \right]^2 + \sum_{i=1}^{N} (k-1) R_{on} \left[\frac{\Delta q_{V_{out}}}{k^{\{-i+(N-1)\}}} \right]^2 + R_{on} \left[\frac{\Delta q_{V_{out}}}{k} \right]^2 \right]. \tag{10}$$

The number of total switches can be expressed as $NK(K+1)+K$. The number of total capacitors can be expressed as $NK+1$.

Based on the above-mentioned theoretical analysis, the theoretical evaluation is conducted concerning the following three samples. The first is the traditional Fibonacci converter with 4 stages shown in Figure 1. The second is the proposed converter-1 shown in Figure 5. The third is the proposed converter-2 shown in Figure 6. From (9) and (10), we derived the characteristics shown in Table 1. As it can be seen from this table, the component count of the traditional converter is smaller than that of the proposed converter. However, the power efficiency of the proposed converters is higher than that of the traditional converter, because the internal resistance of the proposed converters is small. Moreover, the voltage gain of the proposed converter-2 is the highest.

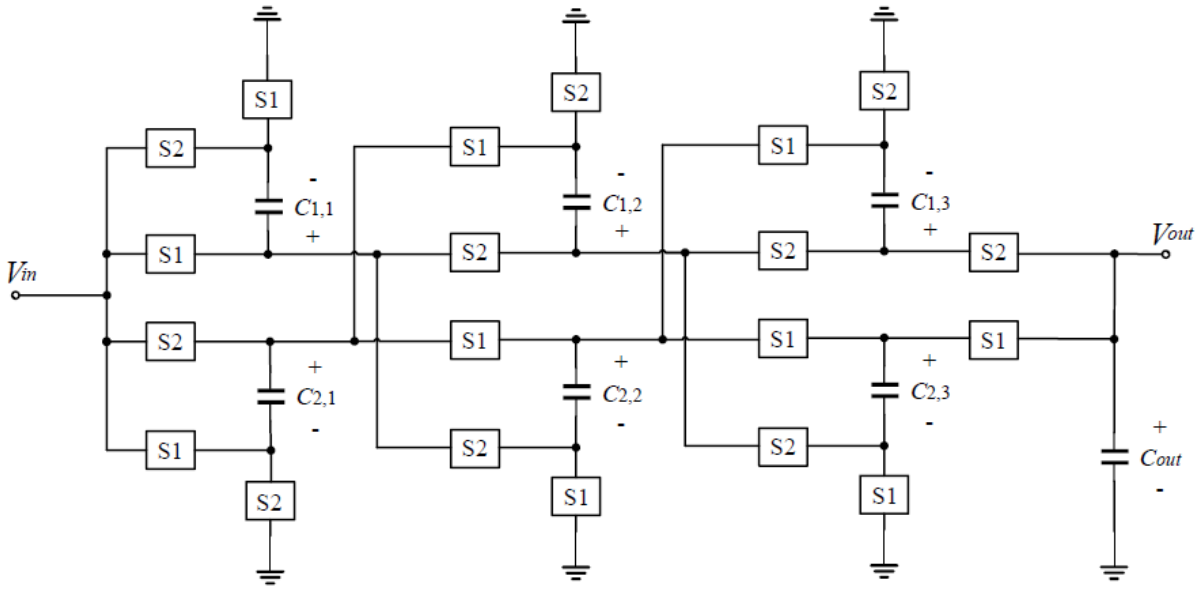

FIGURE 5. Circuits configuration of the proposed converter-1 (2 blocks with 3 stages)

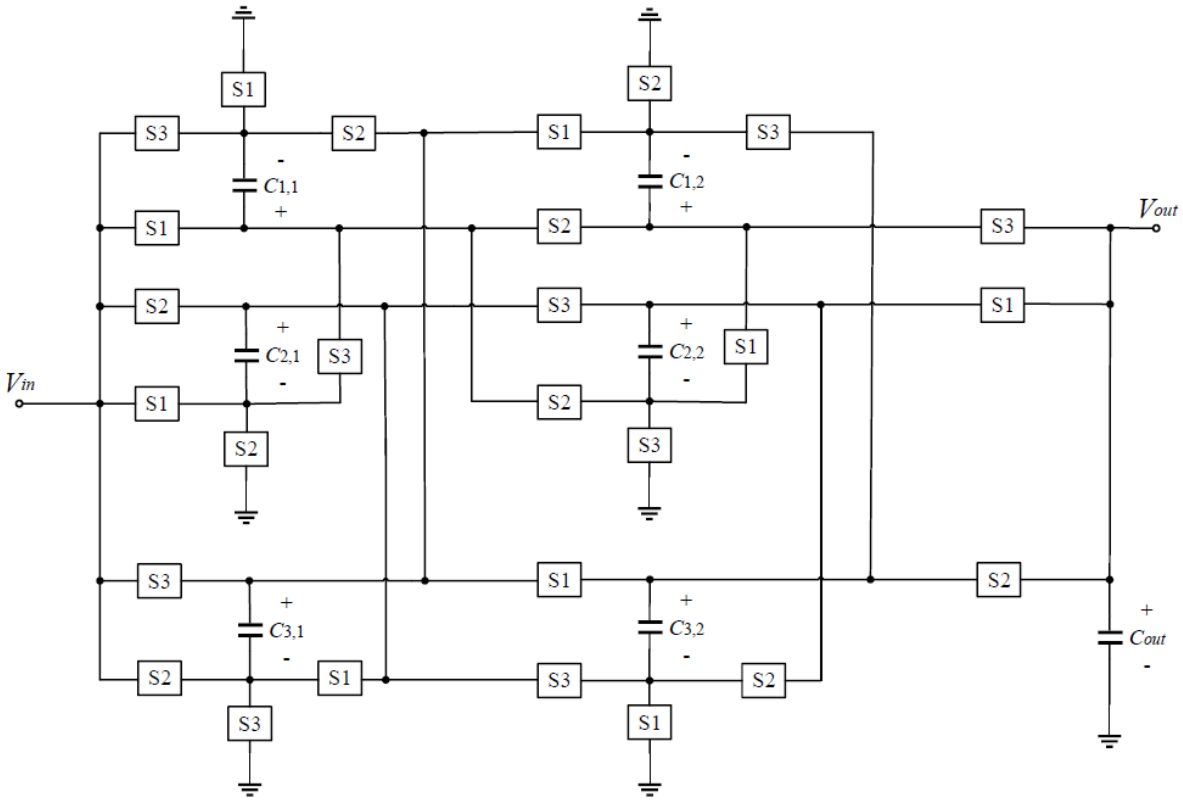

FIGURE 6. Circuits configuration of the proposed converter-2 (3 blocks with 2 stages)

TABLE 1. Comparison of the number of circuit components and characteristic

Type	Number of switches	Number of capacitors	Voltage gain	Power efficiency $\eta_{\max}$
Fibonacci converter	13	5	7	$R_L/(140R_{on} + R_L)$
Proposed converter-1 (2 blocks with 3 stages)	20	7	7	$R_L/(64R_{on} + R_L)$
Proposed converter-2 (3 blocks with 2 stages)	27	7	9	$R_L/(101R_{on} + R_L)$

4. **Experimental Results.** To confirm the feasibility of the proposed topology, some experiments were conducted. In the performed experiments, the conditions are as follows: the input voltage $V_{in} = 400$ mV, the capacitors $C_{1,1} = C_{1,2} = C_{1,3} = 4.7$ µF, $C_{out} = 4.7$

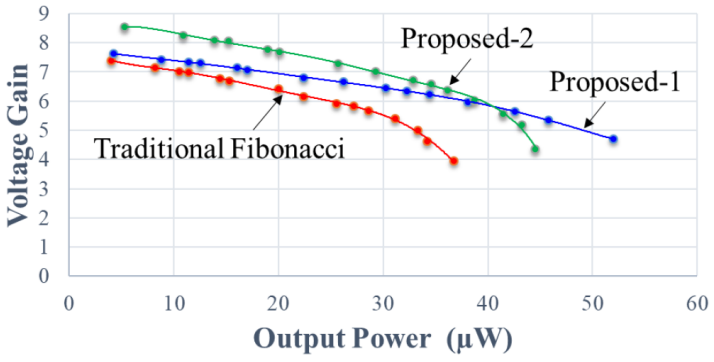

FIGURE 7. Measured voltage gain

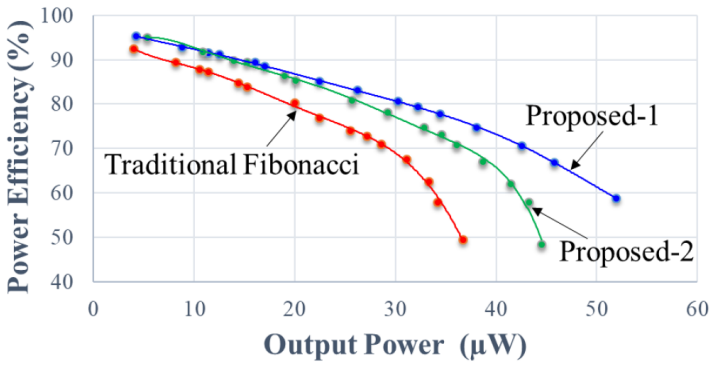

FIGURE 8. Measured power efficiency

μF, and 22 μF, the clock frequency $f = 50$ Hz, the output load $R_L = 68$ kΩ – 2.2 MΩ. Figure 7 demonstrates the comparison in voltage gains. As it can be seen from Figure 7, the voltage gain of the proposed converter-2 is the highest. Figure 8 shows the comparison in power efficiency. As it can be seen from Figure 8, the proposed converter-1 can achieve the highest power efficiency.

5. **Conclusions.** In this paper, we proposed a Fibonacci parallel-connected SC DC-DC converter for energy harvesting systems. The results of theoretical analysis and experiments revealed the effectiveness of the proposed converter. The results of this work are as follows: 1) The proposed converter can realize high voltage gain and is flexible to design with K^N voltage gain, 2) The power efficiency of the proposed converter is higher than that of the traditional converter, because the proposed converter has a small internal resistance, 3) Owing to the symmetrical topology, the proposed converter can reduce the size of output capacitor. From these results, energy harvesting systems will be more efficient by using the proposed converter that has high voltage gain, high power efficiency and small size.

In a future study, we are going to experiment with the conditions of the same integrated circuit for the design of high-efficiency converter chips.

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