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A RESET TYPE 2-MODE DIGITAL FLL WITH ANTI-PSEUDO-LOCK FUNCTION AND PHASE CONTROL

Mitsutoshi Yahara[1], Kuniaki Fujimoto[2] and Daishi Nishiguchi[2]

[1]Department of Medical Care and Welfare Engineering
[2]Department of Electronics and Intelligent Systems Engineering
Tokai University
9-1-1, Toroku, Higashi-ku, Kumamoto-shi, Kumamoto 862-8652, Japan
{ yahara; fujimoto }@tokai.ac.jp

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Abstract. *In the clock generator for clock distribution for driving each system of the mobile communication device, it is desirable to quickly recover from the stopped state and to supply a stable clock from the viewpoint of low power consumption. In this paper, we propose the reset type 2-mode digital frequency-locked loop (FLL) with anti-pseudo-lock function and phase coincidence control. When this FLL falls into anti-pseudo-locked state, it can detect this state and can return to the normal locked state. Also, it is possible to detect the phase error between the input and the output signals in the frequency-locked state, and make these phases coincide. In addition, the initial pull-in can be finished in 1 period of the input signal.*
Keywords: Frequency-locked loop, Pseudo-lock, Phase control, PLL

1. **Introduction.** With the rapid development of the IoT (Internet of Things) society, mobile communication devices are playing an increasingly important role. Also, their functions have diversified in recent years. For this reason, in addition to a clock signal generator that drives itself, a microprocessor incorporated in a mobile communication device has a plurality of clock signal generators for distributing clocks for driving other circuits on the system, and it is synchronized with the external system. Figure 1 shows the configuration. In the mobile communication device, since the standby state is extremely long, the power consumption in that state greatly affects the power consumption of the entire system from the viewpoint of the battery life. Therefore, if it is possible to stop the clock generation circuit during standby and stop the clock supply to the system, not only the power consumption of each system, but also the power consumption related to the clock signal generator can be reduced [1]. However, when the system returns from the standby state, the quick supply of the clock signal becomes a very important matter which affects the performance of the entire system.

One of commonly used circuits in clock signal generators is a phased-locked loop (PLL) [2]. PLL is a circuit that outputs signals with same phase and frequency as input signal. This circuit is used in a wide range of fields including a frequency synthesizer, demodulation of various signals, rotation control of a motor, and the like. However, since the PLL requires lock of frequency and phase before an input signal is added and an output clock is generated, the PLL needs a long time to stabilize the output clock. As a result, the PLL cannot recover quickly from the stopped state, and has problems in using it as a clock distribution circuit in the system. Studies on all digital PLLs have also been performed, but the pull-in time has not been extremely improved, and the lock-in range is also extremely narrow, so designing according to the application is required [3-5].

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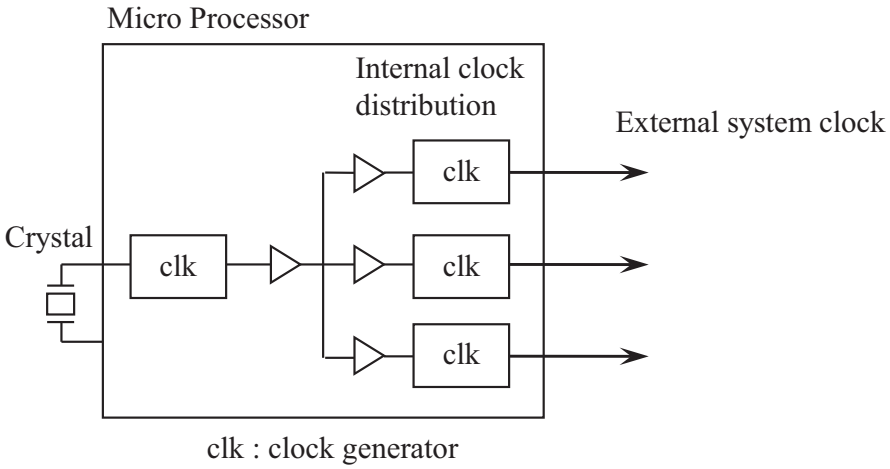

FIGURE 1. Example of clock distribution system

On the other hand, a frequency-locked loop (FLL) is a clock signal generator which does not require the phase control. The FLL is a circuit that generates a clock locked only the frequency for the input signal, and the phase is not locked. Consequently, it is possible to shorten the time until clock generation compared to the PLL. Also, it can be realized stable operation even if there are discontinuous points in the phase of the input signal without being affected by the clock propagation delay [6,7]. However, in the conventional FLL, since it was difficult to construct a frequency comparator which detected a frequency error at a high speed and accurately, it had a problem that the frequency of the output signal could not be accurately obtained.

In order to solve the above problems, the authors previously proposed the 2-mode all digital FLL (DFLL) that realizes a very accurate frequency of an output signal and fast initial pull-in for input signal [8]. The initial frequency pull-in of this DFLL is 1 cycle of the input signal. Also, even when a cycle slip occurs between the input and the output signals, it is possible to obtain an output signal with stable low output jitter without being affected by the cycle slip. However, it had the problem of falling into a pseudo-locked state in which the frequencies of the input and the output signals were locked while maintaining the relationship of $1 : n$ (n is an integer excluding 1). In addition, since the DFLL was unlocked the phase, the phase difference between the input and the output signals always occurred, so that it was difficult to adjust the timing between the systems when used as a clock distribution circuit in the system.

In this paper, we propose a reset type 2-mode digital FLL with an anti-pseudo-lock function and a phase coincidence detection circuit for solving the conventional DFLL. The proposed DFLL detects this when it falls into a pseudo-lock and can return to the normal locked state. Also, after frequency-locked, the phases between the input and the output signals can be agreed by detecting the phase error and resetting the counter for generating the output signal. Furthermore, the characteristics of the DFLL of [8] previously proposed are inherited with respect to the frequency error, the initial pull-in time, and the cycle slip correspondence between the input and the output signals.

In Chapter 2, we describe the circuit configuration and the basic operation of the proposed DFLL. In Chapter 3, we describe the anti-pseudo-lock function and the phase coincidence control. In Chapter 4, we show the simulation results by Verilog-HDL. Finally, Chapter 5 is a conclusion.

2. Proposed 2-Mode Digital FLL with Anti-Pseudo-Lock Function and Phase Control.

2.1. **Circuit configuration of proposed DFLL.** Figure 2 shows the circuit configuration of proposed 2-mode DFLL with anti-pseudo-lock function and phase coincidence detection circuit. Here, FC is the digital frequency comparator corresponding to cycle slip. FC outputs not only the frequency error of the input and the output signals as a digital value but also the lead or the lag signals of the phase. The FER is the adjustment circuit for removing the frequency error between the input and the output signals from the output signal. Divider is the variable frequency divider which divides the reference clock according to the value of FER and generates an output signal. FFP is the fast frequency pull-in circuit that realizes 2-mode operation by improving the frequency pull-in characteristic at the time when an input signal is added. The APF is a circuit for restarting the FEP when the loop falls into the pseudo-locked state and returning to the normal locked state. PCC is the phase error detection circuit for detecting and removing the phase error between the input and the output signals in the frequency-locked state. fx is the reference clock source for controlling the loop. Also, "O", "P" and "Q" are each output points internal circuit of the FC shown in Figure 3.

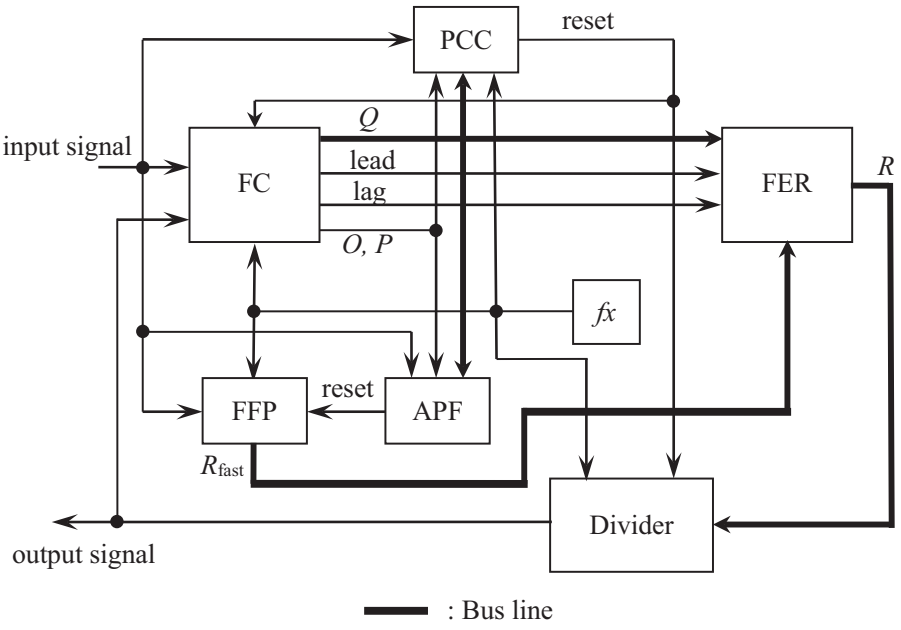

FIGURE 2. Circuit configuration of proposed 2-mode digital FLL

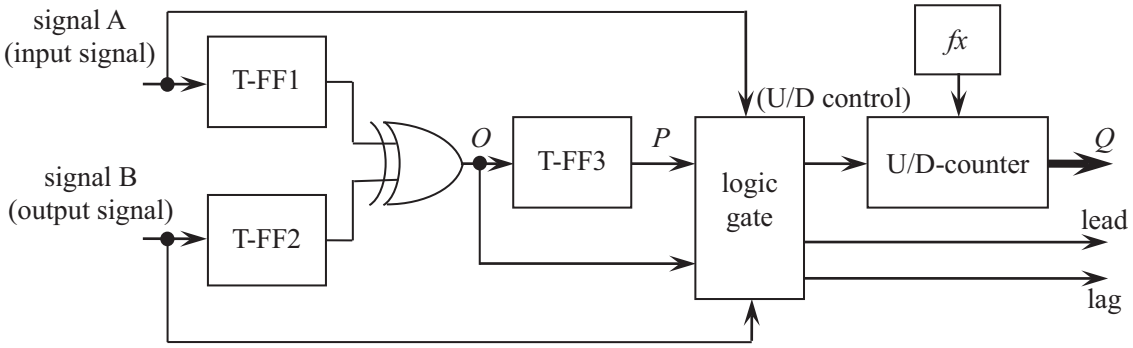

FIGURE 3. Circuit configuration of digital frequency comparator in Figure 2

2.2. **Basic operation of proposed DFLL.** Figure 3 shows the circuit configuration of the proposed digital frequency comparator corresponding to the cycle slip in Figure 2. In this circuit, the pulse at point "O" corresponding to the frequency error is configured to be inverted at rising edge of either the input signals A or B (output signal of DFLL). The reason for this is to detect an appropriate frequency error even when the cycle slip occurs between the input signals A and B.

Next, we explain the detection operation of frequency error. In the state I of Figure 4, U/D-counter up-counts the reference clock number that passes while the point "O" is at the high level, from the initial value "X". Assuming that the reference clock number (up-count value) passing while the state I is "Y", the count value "Q" of U/D-counter is "$X + Y$" at the end of state I.

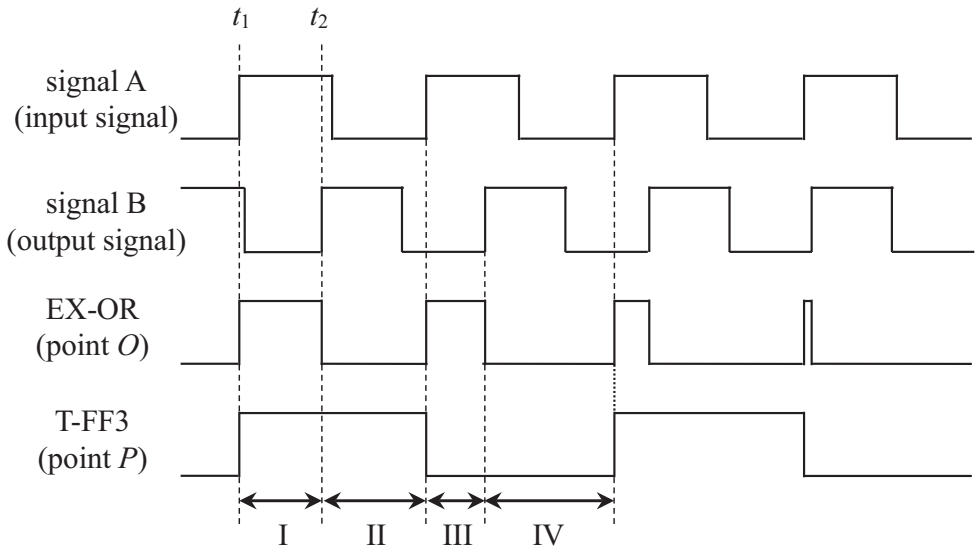

FIGURE 4. Waveforms of digital frequency comparator

In the state II, the count value "Q" is held.

In the state III, U/D-counter down-counts the reference clock number that passes while the point "O" is at the high level. Assuming that the reference clock number (down-count value) passing while the state III is "Z", the count value "Q" is "$X + Y - Z$". As a result, the count value "Q" becomes a value corresponding to the frequency error between input signals A and B at the end of state III.

In the state IV, the count value "Q" is transferred to FER of the next stage. If the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y > Z$", FER decreases the output value which becomes the dividing ratio "R" of divider by the value corresponding to the frequency error. When the dividing ratio before state IV is "R_{pre}", the dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} - (Y - Z) \tag{1}$$

As a result, the output frequency of the proposed DFLL increases according to the difference between "Y" and "Z", so that it operates to remove the frequency error between input and output signals.

Conversely, if the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y < Z$", FER increases the output value by the value corresponding to the frequency error. The dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} + (Z - Y) \tag{2}$$

As a result, the output frequency of the proposed DFLL decreases according to the difference between "Y" and "Z", so that it performs the same removing operation. Also,

TABLE 1. Control state of dividing ratio according to the phase lead or lag

	state I	state III	Equation (1)	Equation (2)
Pattern 1	lead	lead	$R = R_{pre} - (Y - Z)$	$R = R_{pre} + (Z - Y)$
Pattern 2	lead	lag	$R = R_{pre} + (Y - Z)$	$R = R_{pre} + (Z - Y)$
Pattern 3	lag	lead	$R = R_{pre} - (Y - Z)$	$R = R_{pre} - (Z - Y)$
Pattern 4	lag	lag	$R = R_{pre} + (Y - Z)$	$R = R_{pre} - (Z - Y)$

the count value "Q" of U/D-counter is set to the initial value "X" for the next count at this time. In addition to this, the dividing ratio "R" is controlled as shown in Table 1 according to the phase lead or lag states between input and output signals.

Next, we consider frequency lock-in range and stationary frequency error of the proposed DFLL. The proposed DFLL is configured to determine the frequency of output signal by dividing the reference clock fx with the dividing ratio "R". Therefore, the frequency lock-in range is determined by the setting range of "R". Here, when the lower limit value of the dividing ratio is "$R_{\min}$" and the upper limit value is "$R_{\max}$", the frequency lock-in range of the proposed DFLL is determined as follows.

$$\frac{f_s}{R_{\max}} \leq f_{in} \leq \frac{f_s}{R_{\min}} \tag{3}$$

where f_{in} is the frequency of input signal and f_s is the frequency of the reference clock. Also, in the steady state, the proposed DFLL occurs a steady frequency error of less than 1 period of the reference clock at the maximum. Therefore, the average frequency f_{avg} of the output signal is expressed as follows.

$$f_{avg} = \frac{\left(\frac{1}{R} + \frac{1}{R \pm 1}\right)}{2} f_s \tag{4}$$

In consequence, if the dividing ratio "R" is set to a certain large value, the influence on the jitter suppression effect by this error is considered to be negligible.

3. **Anti-Pseudo-Lock and Phase Coincidence Control.**

3.1. **Anti-pseudo-lock function.**

The pseudo-lock is a phenomenon in which the frequencies of the input and the output signals are locked while maintaining the relationship of $1 : n$, depending on the delay time of the DFLL, the frequency characteristic of the divider, the phase state, and the like. In the conventional DFLL, if it falls into this state, the control in the loop becomes equivalent to that in the normal locked state, so it was not possible to recover to the normal locked state. Therefore, in the frequency-locked state of the proposed DFLL, we focused on the fact that the value "Q" of the U/D-counter constituting the FC becomes the initial value "X" at the time of the state IV in Figure 4, so that this DFLL can be recovered to the normal locked state.

The upper side of the broken line in Figure 5 shows the anti-pseudo-lock circuit in the proposed DFLL. This circuit is composed of a counter (counter1), two digital comparators (DC1, DC2), a selector (sel), NOR gate, and AND gate. DC1 compares the value "Q" of the U/D-counter in the FC in the state IV of Figure 4 and its initial value "X". In the pseudo-locked state, since "Q" at the time of transfer to FER is the initial value "X", DC1 outputs a high level when it satisfies the relation of "$Q = X$". DC2 compares "2" with the value "Z" of the counter1 which counts the output signal during 1 period of the input signal. Since the clock number of the output signal generated in 1 period of the input signal is 2 clocks or more, DC2 becomes high level when satisfying the relation of "Z" ≥ 2. This circuit can detect that the pseudo-locked state has occurred at the time when both DC1 and DC2 are at the high level. Therefore, its circuit returns the proposed

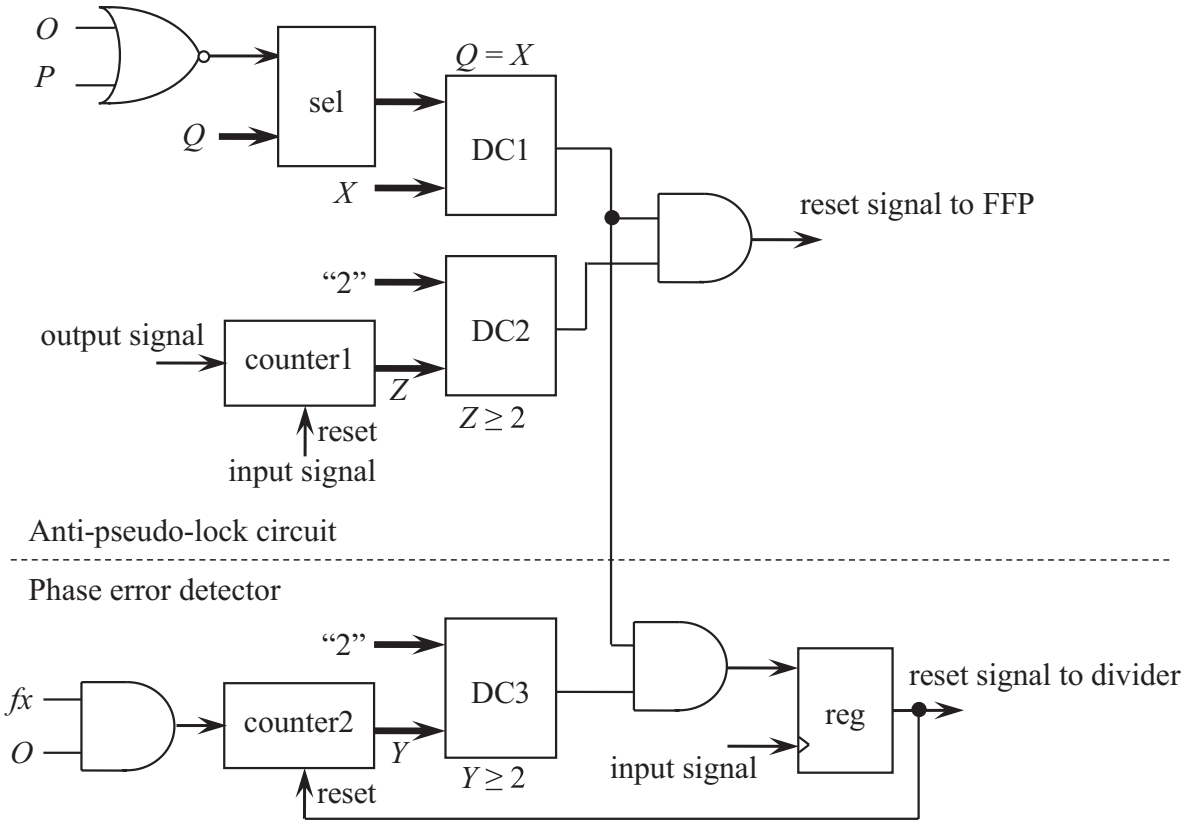

FIGURE 5. Circuit configuration of anti-pseudo-lock circuit and phase error detector

DFLL from the pseudo-locked state to the normal locked state by restarting the initial pull-in circuit with the reset signal through the AND gate.

3.2. **Phase coincidence control.** Since the DFLL locks only the frequencies of the input and the output signals, the phase difference between 2 signals always occurs. However, when used as a clock distribution circuit in the system, it is desirable that the phases of the input and the output signals are in agreement in consideration of lock between the processor and the external system. Therefore, in the frequency-locked state of the proposed DFLL, we focused on the fact that the value "Q" of the U/D-counter constituting the FC becomes the initial value "X" as described above, and remove it by detecting the phase error in this state.

The lower side of the broken line in Figure 5 shows the phase error detector in the proposed DFLL. This circuit is composed of a counter (counter2), a digital comparator (DC3), AND gate, register (reg) in addition to the output of DC1 of the anti-pseudo-lock circuit. DC3 compares "2" with the value "Y" of the counter2 which counts the reference clock while the point "O" of the FC is at the high level. Considering that the frequency error in the steady state of this DFLL is Equation (4), when the phase error between the input and the output signals occurs, the value of the counter2 is "2" or more. In consequence, the DC3 outputs a high level at the time when the relation of "Y" ≥ 2 is satisfied. This circuit can detect the phase error between the input signal and the output signal in the frequency-locked state when DC1 and DC3 are both at the high level. Therefore, the proposed DFLL can remove the phase error between the input and the output signals by resetting the divider with the signal from the register at the rising edge of the input signal.

4. **Simulation Results.** This simulation was described using Verilog-HDL as hardware description language.

Figure 6 shows the simulation waveforms of each part of the conventional DFLL. From this, it is found that the dividing ratio "R" that determines the frequency of output signal operates within the range satisfying Equation (4). However, the phase between the input and the output signals has locked with the error.

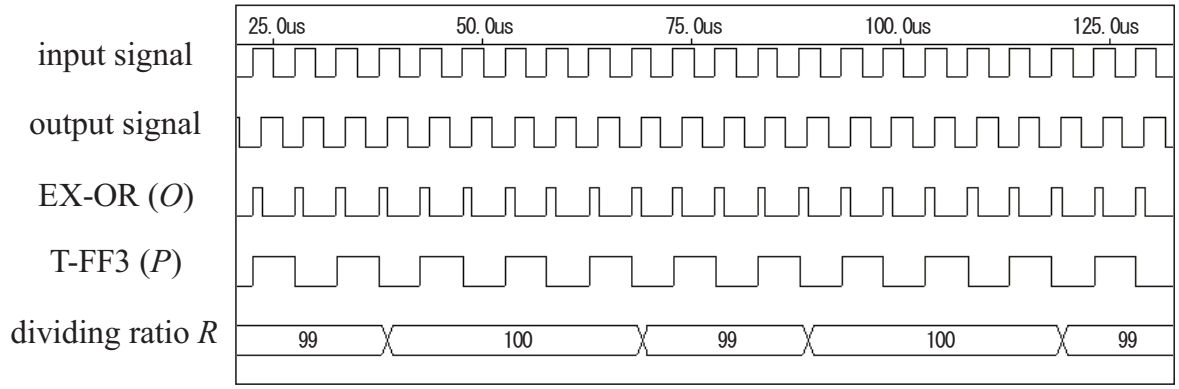

FIGURE 6. Simulation waveforms of conventional DFLL

Figure 7 shows the simulation waveforms of each part of the proposed DFLL using the phase coincidence control. From this, it is found that the proposed DFLL detects the phase error between the input and the output signals at time t_0, and removes it by resetting the divider at time t_1.

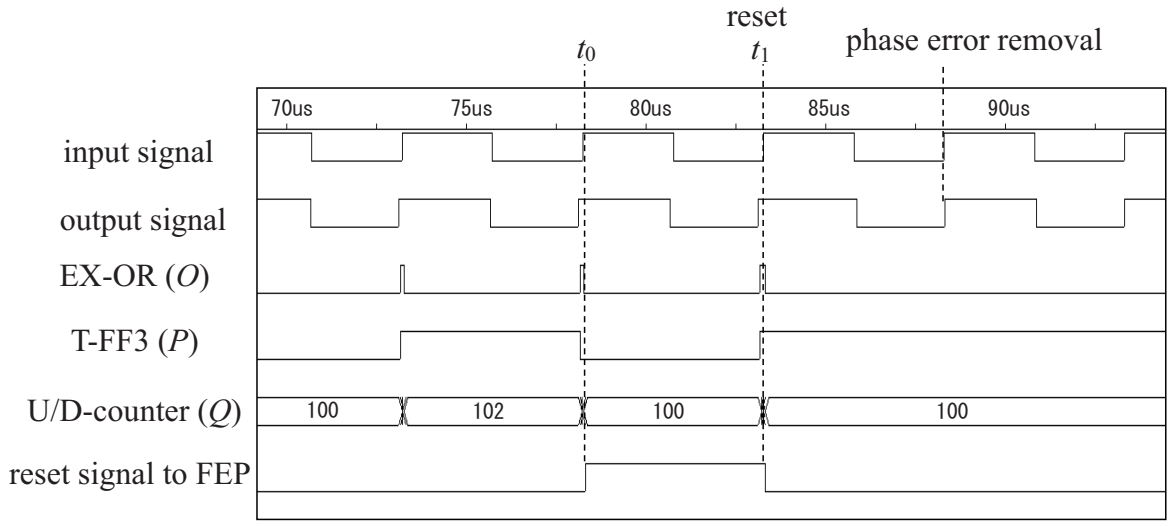

FIGURE 7. Simulation waveforms of proposed DFLL using phase coincidence control

Figure 8 shows the simulation waveforms of each part of the proposed DFLL using the anti-pseudo-lock function. From this, although the proposed DFLL falls into the pseudo-locked state at time t_0, it is found that the anti-pseudo-lock function operates at time t_1 and returns to the normal-locked state at time t_2.

5. **Conclusion.** In this paper, we proposed the reset type 2-mode digital FLL with anti-pseudo-lock function and phase coincidence control. This DFLL detects this when falling into the pseudo-locked state and can return to the normal locked state by resetting the loop. Also, it is possible to detect the phase error between the input and the output signals after the frequency locked and remove the phase error. In addition, we confirmed that it inherits the characteristics of the DFLL of [7] previously proposed in respect to

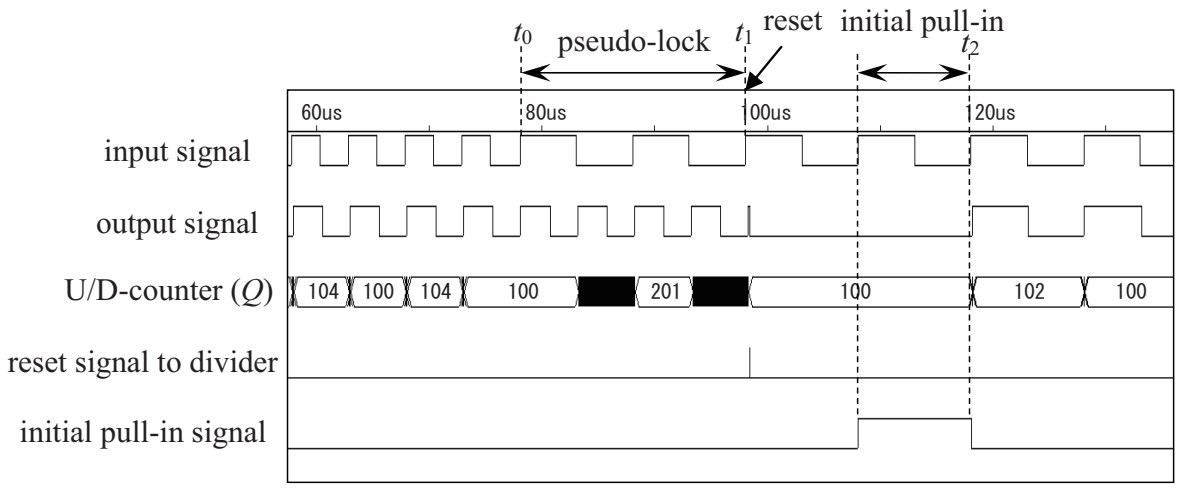

FIGURE 8. Simulation waveforms of proposed DFLL using anti-pseudo-lock function

the frequency error, the initial pull-in time, and the cycle slip correspondence between the input and the output signals.

In the future, we plan to examine the configuration to further reduce stationary frequency error.

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