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SHORT-CIRCUIT-CURRENT REDUCTION BY USING A CLOCKED NEURON CMOS INVERTER IN A TIME-DOMAIN DATA COINCIDENCE DETECTOR

Masaaki Fukuhara[1], Nao Onji[1], Takanori Kurano[1], Tasuku Nakajima[1]
Yujiro Harada[2], Kuniaki Fujimoto[2] and Masahiro Yoshida[1]

[1]Department of Embedded Technology
School of Information and Telecommunication Engineering
Tokai University
2-3-23, Takanawa, Minato-ku, Tokyo 108-8619, Japan
fukuhara@tokai.ac.jp

[2]Graduate School of Science and Technology
Tokai University
9-1-1, Toroku, Higashi-ku, Kumamoto 862-8652, Japan
fujimoto@tokai.ac.jp

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Abstract. *A data coincidence detector with a neuron CMOS (Complementary Metal-Oxide-Semiconductor) inverter can detect Hamming distance between two input data in time domain. In the detector, a short-circuit-current flows continuously during Hamming distance search operation since the neuron CMOS inverter of the detector behaves around the inversion threshold voltage. To solve this problem, we propose a new data coincidence detector using a clocked neuron CMOS inverter. In this paper, operating algorithm of the proposed detector is described, and the characteristics of short-circuit-current and power consumption of the proposed detector are verified by HSPICE which is one of the most standard analog circuit simulators. By using clocked neuron CMOS inverter and reducing short-circuit-current, power consumption at the neuron CMOS inverter of the proposed detector is down to about 8% compared with a conventional data coincidence detector.*

Keywords: Clocked CMOS, Neuron CMOS inverter, Short-circuit-current, Power consumption

1. **Introduction.** A neuron MOS transistor or a neuron CMOS inverter can calculate the weighted sum of multiple input voltages and behave the threshold operation like a neuron [1]. A data coincidence detector using the neuron CMOS inverter mentioned above outputs a signal with time delay corresponding to a Hamming distance between two input data: DATA-A and DATA-B [2]. The detector is useful for an associative memory or a CAM (Content Addressable Memory) which can perform a fuzzy search at high speed and can discriminate in time domain if the Hamming distance between an input-data word and reference-data words is within a certain range or not. Therefore, the CAM with the Hamming distance search function or the detector retrieves the most similar data and is useful for many applications including pattern recognition and fingerprint recognition [3].

In the neuron CMOS inverter of the conventional data coincidence detector [2], a large quantity of short-circuit-current flows since the floating gate voltage behaves around the inversion threshold voltage of the neuron CMOS inverter.

In Section 2 of this paper, we propose a new data coincidence detector to reduce the short-circuit-current by utilizing a clocked neuron CMOS inverter [4-6]. In Section 3, to clarify the characteristics of short-circuit-current and power consumption, HSPICE simulations are performed of the proposed detector designed by Hibikino 2μm CMOS

process design rule. Finally, we describe that the proposed detector operates at low power of about 50% compared to conventional detector and summarize this paper in Section 4.

2. Proposed Circuit.

2.1. Circuit configuration.

Figure 1 illustrates the circuit configuration of the proposed data coincidence detector with a clocked neuron CMOS inverter, and Figure 2 shows the equivalent circuit of the proposed detector.

The proposed detector consists of EXclusive-OR (EXOR) Gate Array (hereafter EXGA), Current Mirror circuit (hereafter CM) and Clocked Neuron CMOS Inverter (hereafter CNCI). Although omitted in Figure 1, all of the substrates of nMOS transistors are connected to *GND*, and all of the substrates of pMOS transistors are connected to V_{DD}.

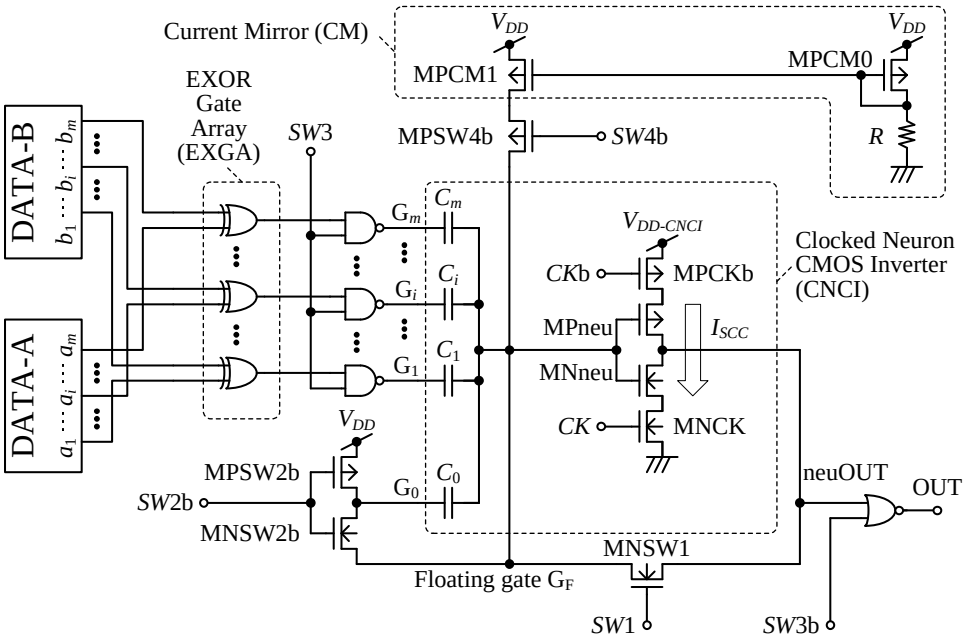

FIGURE 1. Circuit configuration of the proposed data coincidence detector

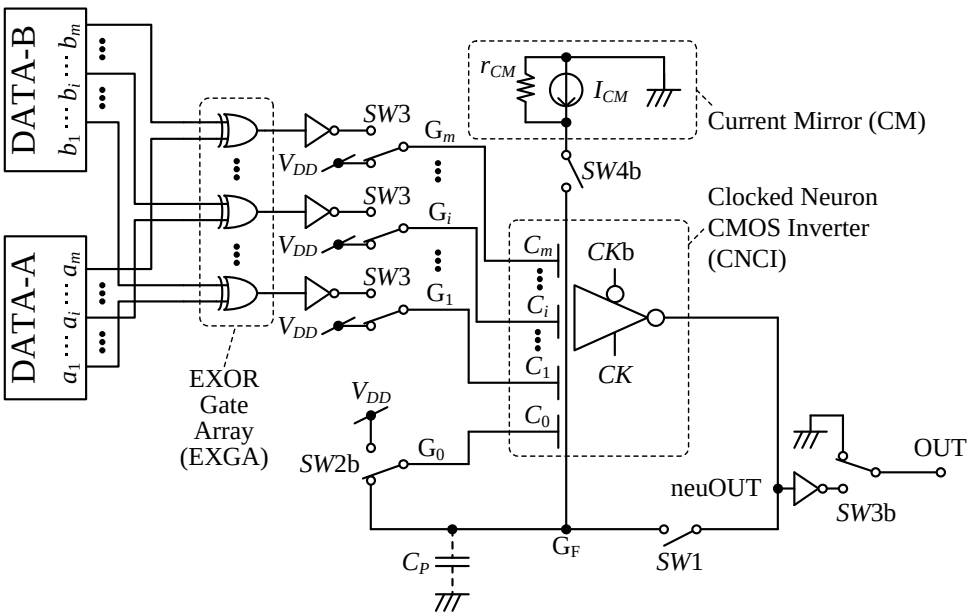

FIGURE 2. Equivalent circuit of the proposed detector

m denotes the bit length of 2 input data DATA-A $(a_1, a_2, \ldots, a_m)$ and DATA-B $(b_1, b_2, \ldots, b_m)$ to be compared in the proposed detector, and then the EXGA has m EXOR gates to decide whether match or mismatch in each bit of the DATA-A and DATA-B.

The CM is constituted by 2 transistors MPCM0 and MPCM1, and a resister R, and supplies a constant current to floating gate $\mathrm{G_F}$ of CNCI. The CM has been rewritten of a constant current source I_{CM} and a drain output resistance r_{CM} in Figure 2. The I_{CM} flows to a parasitic capacitor C_P through the floating gate, and floating gate voltage $V(\mathrm{G_F})$ changes to a voltage corresponding to the Hamming distance D_H between DATA-A and DATA-B in data coincidence operation. Here, Hamming distance D_H means the number of different bits between two data, and is expressed as

$$D_H = \sum_{i=1}^{m} (a_i \oplus b_i), \tag{1}$$

where $\oplus$ is an EXOR (EXclusive-OR) operator. A range of D_H is from 0 to m.

The CNCI consists of a neuron CMOS inverter (MNneu and MPneu) with 2 transistors (MNCK and MPCKb) to be controlled by clock signals *CK* and *CK*b and to reduce the short-circuit-current. The neuron CMOS inverter has a floating gate $\mathrm{G_F}$, $(m+1)$ input gates G_i $(i = 0, 1, 2, \ldots, m)$ and $(m+1)$ capacitors C_i $(i = 0, 1, 2, \ldots, m)$. Because the weight of each bit is equal in calculating the Hamming distance, the capacitances are designed as follows:

$$C_0 = C_1 = C_2 = \cdots = C_m \equiv C. \tag{2}$$

In Figure 1 and Figure 2, V_{DD} is the power supply voltage and *GND* means the voltage of ground level (0[V]). In this paper, it is written as HIGH or LOW when the voltage is V_{DD} or *GND*. $V_{DD\text{-}CNCI}$ is equal to the power supply voltage and is isolated from V_{DD} because of measuring the short-circuit-current (hereafter I_{SCC}) of CNCI.

This detector has 5 type switches or control signals. *SW*1 switches to equalize $V(\mathrm{G_F})$ to the inversion threshold voltage V_{INV} or to separate $V(\mathrm{G_F})$ from the voltage of output terminal V(neuOUT). *SW*2b is a switch to change whether $V(\mathrm{G_0})$ is connected to $V(\mathrm{G_F})$ or V_{DD}. *SW*3 and *SW*3b are control signals to start data coincidence operation. *SW*4b controls to flow I_{CM}. *CK* and *CK*b are clock signals to control CNCI and to suppress I_{SCC}.

2.2. **Operating principles.** Figure 3 illustrates the waveforms of the input signals, control signals and terminal voltages. Before into Phase 1, *SW*1, *SW*3 and *CK* are LOW, and *SW*2b, *SW*3b, *SW*4b and *CK*b are HIGH. The detector behaves from Phase 1 to Phase 5. We describe each phase separately as below.

<Phase 1>: *CK* rises to HIGH and *CK*b downs to LOW, and then the CNCI is "ON". *SW*1 turns to HIGH, and then the nMOS transistor MNSW1 is "ON". The $\mathrm{G_F}$ is connected to neuOUT, and then $V(\mathrm{G_F})$ and V(neuOUT) are expressed by

$$V\left(\mathrm{G_F}\right)\big|_{\mathrm{Phase1}} = V\left(\mathrm{neuOUT}\right) = V_{INV} \approx \frac{V_{DD}}{2}. \tag{3}$$

*SW*2b keeps HIGH, and then $V(\mathrm{G_0}) = V(\mathrm{G_F}) = V_{INV}$. *SW*3 is LOW, and then each of the $V(\mathrm{G}_i)$ $(i = 1, 2, \ldots, m)$ is V_{DD}. *SW*3b is HIGH, and then the output voltage V(OUT) becomes *GND*. *SW*4b keeps HIGH and the pMOS transistor MPSW4b is "OFF", and then the current I_{CM} does not flow.

<Phase 2>: *SW*1 is dropped on *GND* and MNSW1 is turned "OFF". By this, $V(\mathrm{G_F})$ is isolated from V(neuOUT) and holds V_{INV}. V(OUT) keeps *GND* since *SW*3b holds HIGH. Furthermore, *CK* is turned LOW and *CK*b is turned HIGH to suppress the flowing of the short-circuit-current I_{SCC}. A time lag between Phase 1 and Phase 3 is needed since *SW*2b requires to be downed after *SW*1 has completely lowered. At the latest, input signals a_i $(i = 1, 2, \ldots, m)$ and b_i $(i = 1, 2, \ldots, m)$ are fixed to HIGH or LOW before into Phase 3.

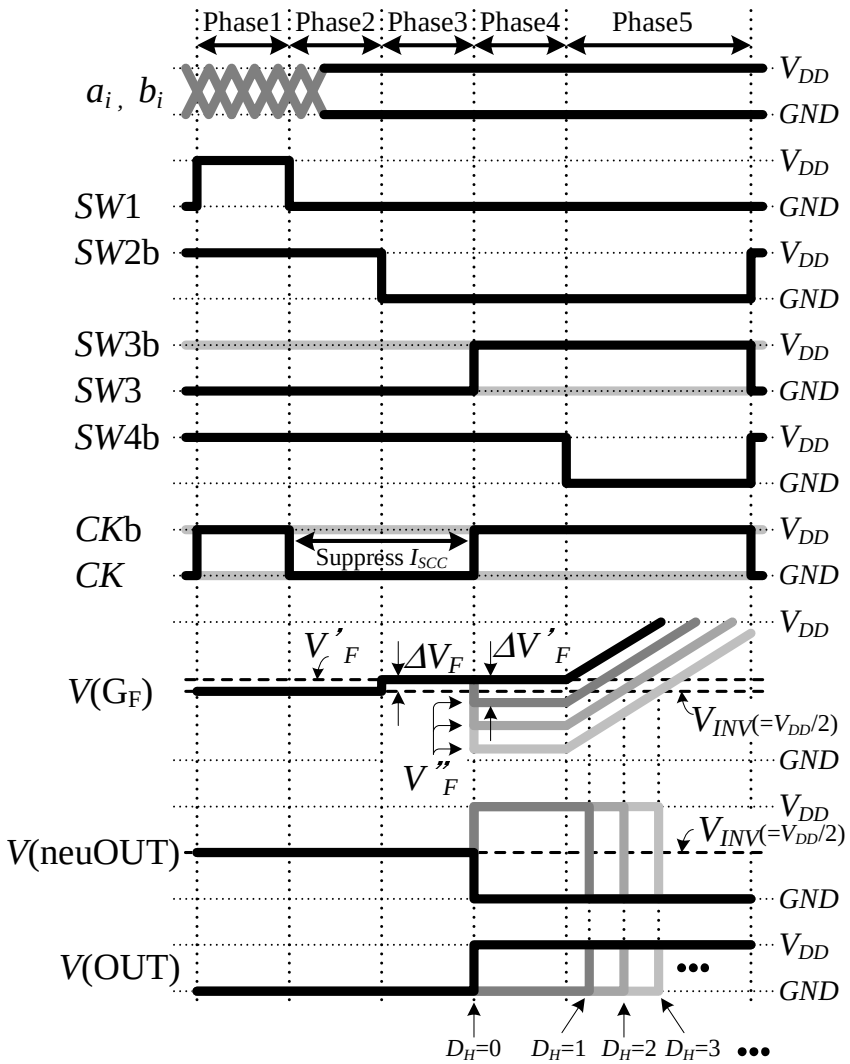

FIGURE 3. Timing chart of control signals and terminal voltages ($i = 1, 2, \ldots, m$)

<Phase 3>: When $SW2$b is turned LOW, $V(\mathrm{G}_0)$ becomes from V_{INV} to V_{DD}. Therefore, the variation of floating gate voltage $V(\mathrm{G_F})$, ΔV_F, is expressed as

$$\Delta V_F = \frac{C_0}{C_{TOT}} \Delta V\left(\mathrm{G}_0\right) = \frac{C}{C_{TOT}}\left(V_{DD} - V_{INV}\right) \approx \frac{C}{C_{TOT}} \cdot \frac{V_{DD}}{2}, \tag{4}$$

where C_{TOT} is the total capacitances on the floating gate and is shown as

$$C_{TOT} = C_0 + C_1 + \cdots + C_m + C_P = (m+1)\, C + C_P. \tag{5}$$

Assuming $C_P \ll C$, the floating gate voltage $V(\mathrm{G_F})$ is given by

$$\begin{aligned} V\left(\mathrm{G_F}\right)\big|_{\mathrm{Phase3}} &= V\left(\mathrm{G_F}\right)\big|_{\mathrm{Phase1}} + \Delta V_F \\ &= V_{INV} + \frac{C}{C_{TOT}} \cdot \frac{V_{DD}}{2} \approx V_{INV} + \frac{1}{m+1} \cdot \frac{V_{DD}}{2} \equiv V'_F. \end{aligned} \tag{6}$$

Since CK and CKb keep the former state, then V(neuOUT) keeps V_{INV} and I_{SCC} has been suppressed. Furthermore, V(OUT) keeps GND since $SW3$b is HIGH.

<Phase 4>: When $SW3$ is set to HIGH, if the Hamming distance D_H between DATA-A and DATA-B is 0, namely, 2 input data are exactly matched, all of the $V(\mathrm{G}_i)$ ($i = 1, 2, \ldots, m$) keep V_{DD}. The floating gate voltage $V(\mathrm{G_F})$ does not change from Phase 3 and is given by

$$V\left(\mathrm{G_F}\right)\big|_{\mathrm{Phase4}, D_H=0} = V'_F = V_{INV} + \frac{1}{m+1} \cdot \frac{V_{DD}}{2}. \tag{7}$$

Equation (7) indicates that the floating gate voltage $V(\mathrm{G_F})$ is higher than the inversion threshold voltage V_{INV}. At the same time, CK rises to HIGH and CKb downs to LOW, and then the MNCK and MPCKb in CNCI become "ON". Therefore, V(neuOUT) becomes LOW and the output voltage V(OUT) becomes HIGH since SW3b is LOW.

On the other hand, if the Hamming distance D_H is larger than 0, namely, 2 input data are unmatched, D_H of the $V(\mathrm{G}_i)$ $(i = 1, 2, \ldots, m)$ are lowered from V_{DD} to GND. The variation of $V(\mathrm{G_F})$ in Phase 4 is defined to $\Delta V'_F$, and then the $V(\mathrm{G_F})$ is expressed as

$$\begin{aligned} V\left(\mathrm{G_F}\right)|_{\mathrm{Phase4},D_H\geq 1} &= V'_F - \Delta V'_F = \left(V_{INV} + \frac{1}{m+1}\cdot\frac{V_{DD}}{2}\right) - \frac{D_H}{m+1}V_{DD} \\ &= V_{INV} - \frac{2D_H - 1}{m+1}\cdot\frac{V_{DD}}{2} \equiv V''_F. \end{aligned} \tag{8}$$

Equation (8) indicates that $V(\mathrm{G_F})$ is lower than V_{INV} when D_H is equal to 1 or more. Therefore, V(neuOUT) becomes HIGH and V(OUT) becomes LOW. As Equation (8) shows, the floating gate voltage V''_F in Phase 4 downs to a voltage corresponding to D_H.

<Phase 5>: When SW4b is changed from HIGH to LOW, the pMOS transistor MPSW4b is switched to "ON" and constant current I_{CM} flows from the CM (Current Mirror) circuit to parasitic capacitor C_P through the floating gate $\mathrm{G_F}$. Therefore, $V(\mathrm{G_F})$ starts to increase linearly from V''_F. When $V(\mathrm{G_F})$ exceeds V_{INV} of CNCI, V(neuOUT) becomes LOW and V(OUT) rises to HIGH. Hence by detecting the "time lag" after SW4b is set to LOW until V(OUT) rises to HIGH, we can know the Hamming distance D_H between DATA-A and DATA-B. [2] describes that the time lag is not affected by the parasitic capacitance and the initial charge, and is invariant to the variation of the threshold voltage caused by the variation of temperature and manufacturing process.

3. Simulated Results.

3.1. Data coincidence operation.

To verify the above operating algorithm of the proposed detector, we carried out the computer simulation HSPICE. Table 1 shows device parameters and simulation conditions.

Figure 4(a) shows the simulated waveforms of clock signal CK (CKb is ignored) and control signals SW1, SW2, SW3 and SW4 (shown instead of SW2b and SW4b). Figure 4(b) shows that the floating gate voltages $V(\mathrm{G_F})$ are voltages corresponding to Hamming distance D_H in Phase 4. Figure 4(c) illustrates that V(OUT) becomes HIGH with a time lag corresponding to D_H. Therefore, the proposed detector in these simulation runs has behaved the data coincidence operation according to the theory mentioned above.

Table 1. Device parameters and simulation conditions

Symbol	Description	Value	Units
V_{DD}	Power supply voltage	5.0	V
GND	Ground voltage	0	V
m	Bit length	4	–
W_n/L_n	Width/Length of nMOS transistor	4.0/2.0	μm
W_p/L_p	Width/Length of pMOS transistor	8.0/2.0	μm
C_i $(i = 0, 1, 2, \ldots, m)$	Capacitance of all of the input gates of CNCI	16	fF
R	Resistance of CM	1.0	KΩ

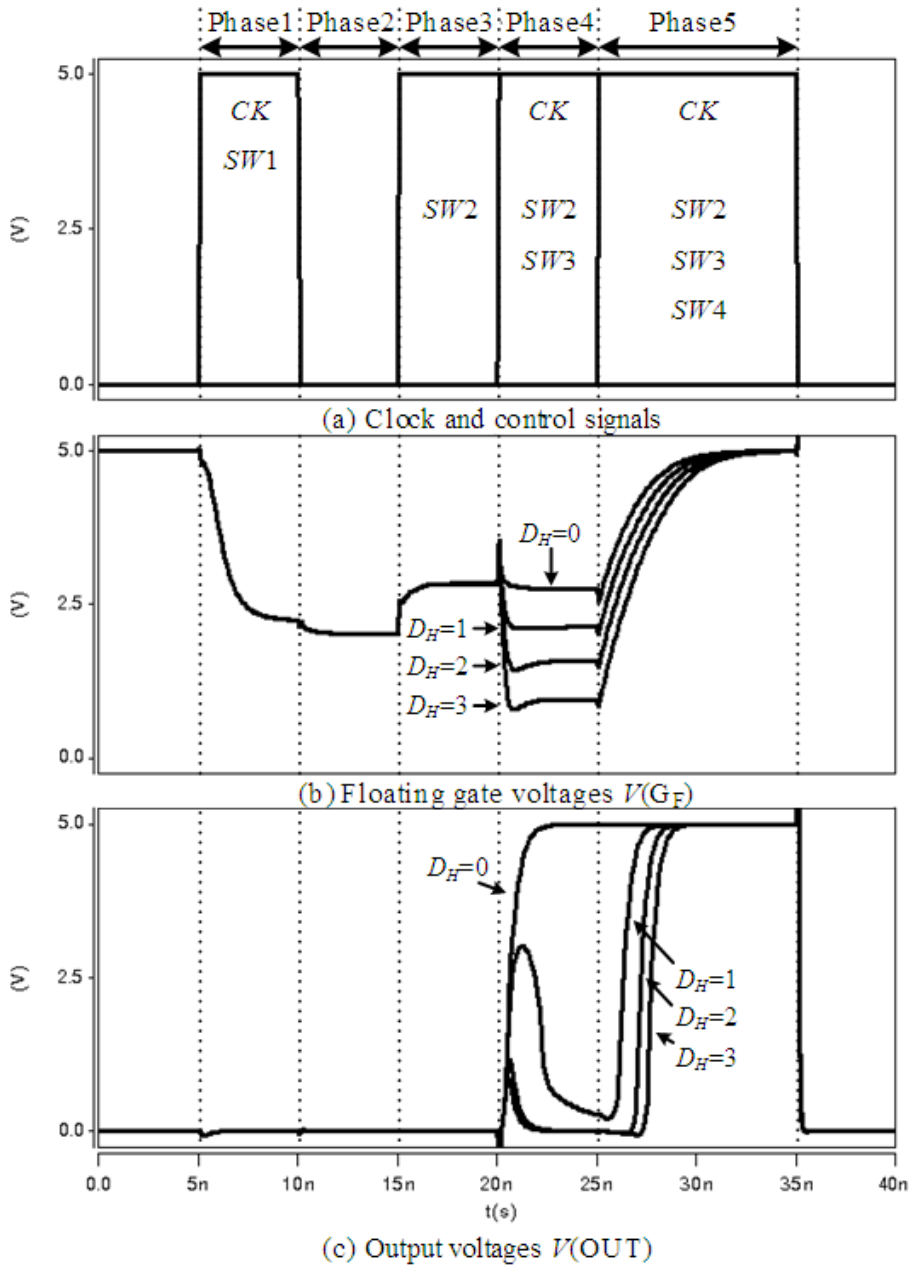

FIGURE 4. Simulated waveforms of control signals, $V(\mathrm{G_F})$ and $V(\mathrm{OUT})$

3.2. **Short-circuit-current.** The simulated waveforms of short-circuit-current (I_{SCC}) at Clocked Neuron CMOS Inverter (CNCI) of conventional detector and the proposed detector are shown in Figures 5(a) and 5(b) respectively. In these simulations, we regard a drain current of MNneu as I_{SCC}. The difference between the proposed detector and conventional one is the presence or absence of a clocked circuit (MNCK and MPCKb). As can be seen from these figures, the wasteful flow of I_{SCC} is suppressed in Phase 2 and Phase 3 by using clocked circuit (MNCK and MPCKb). Since the inversion threshold voltage V_{INV} is adjusted to the floating gate voltage $V(\mathrm{G_F})$ in Phase 1 and since V(neuOUT) is set according to the $V(\mathrm{G_F})$ in Phase 4 and Phase 5, the clocked circuit (MNCK and MPCKb) must be "ON" and *CK* must be HIGH.

3.3. **Power consumption.** Figure 6 shows power consumption at only CNCI by measuring voltage, current and power of $V_{DD\text{-}CNCI}$ in HSPICE simulations. Bit length m is 4, 8, 16 and 32. The power consumption is down to about 50% at CNCI (Clocked Neuron CMOS Inverter).

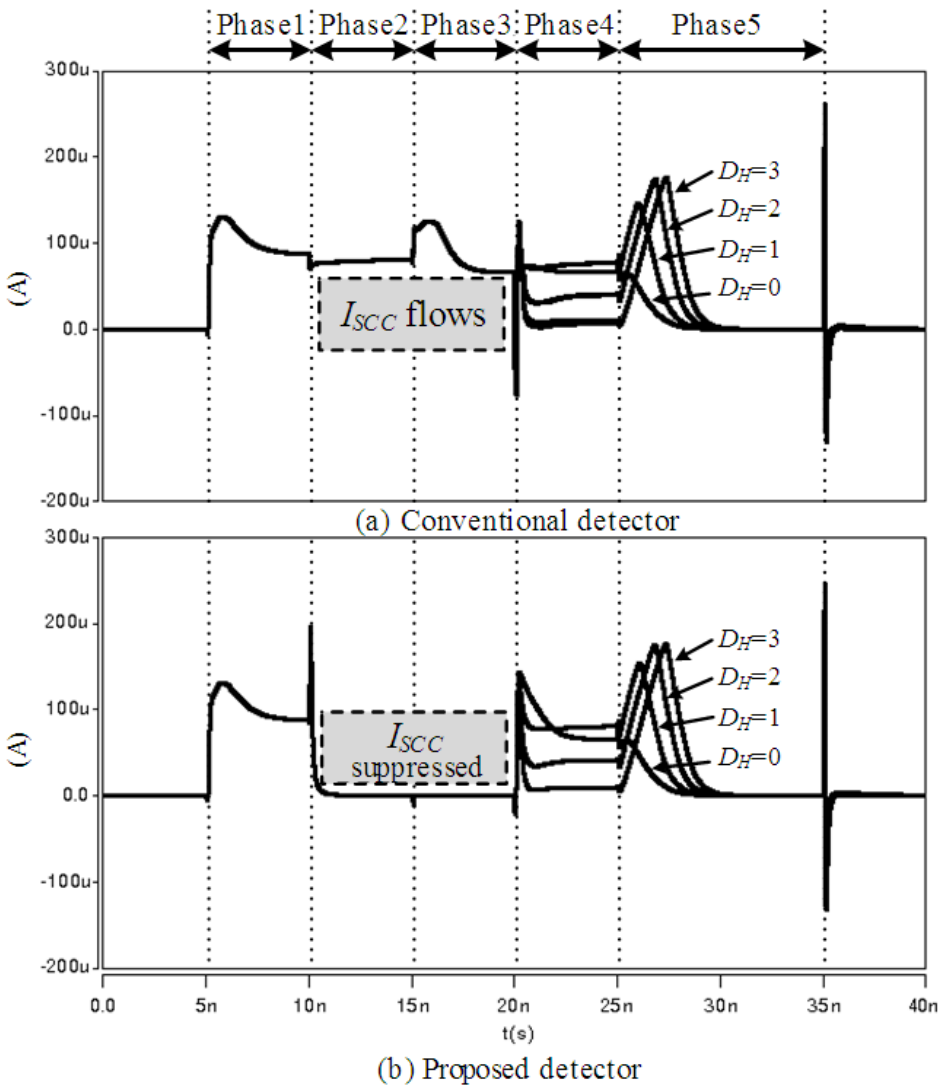

FIGURE 5. Simulated waveforms of I_{SCC}

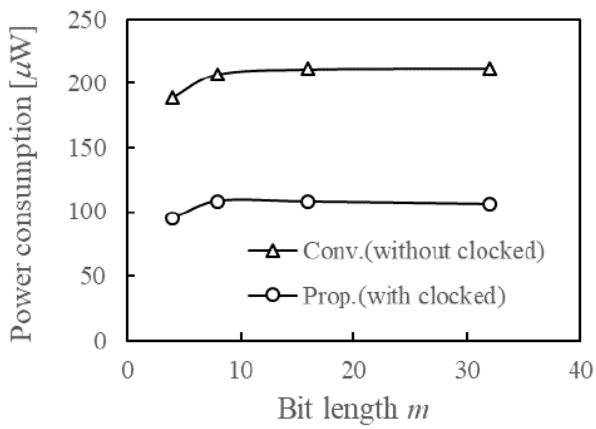

FIGURE 6. Power consumption of only CNCI

Figure 7 shows power consumption of whole detector. From this figure, we know that the power consumption of the proposed detector is down to about 8% compared by conventional detector.

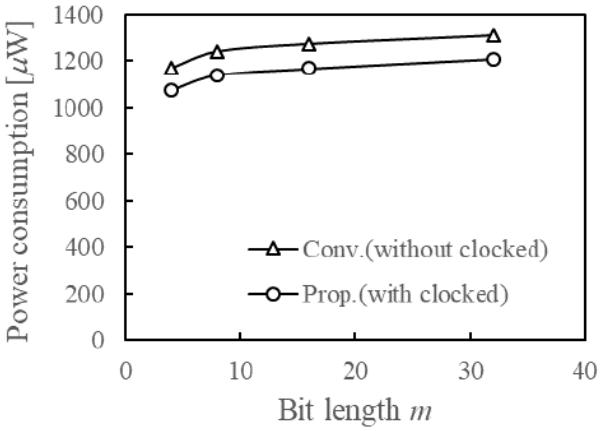

FIGURE 7. Power consumption of whole detector

4. **Conclusions.** This paper has proposed and discussed a data coincidence detector with clocked neuron CMOS inverter. By reducing the waste of short-circuit-current, the proposed detector can reduce the power consumption about 8% compared with conventional detector. In future work, the proposed CNCI is applied to CAM.

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