ICIC Express Letters
Part B: Applications
Volume **9**, Number **12**, December **2018**

 ISSN 2185-2766
pp. **1233–1240**

A DIGITALLY CONTROLLED OSCILLATOR USING 1+1/k FREQUENCY DIVIDER BASED ON MULTI-PHASE CLOCK

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Received May 2018; accepted August 2018

Abstract. *In this paper, we proposed the digitally controlled oscillator using 1+1/k frequency divider based on multi-phase clock. The oscillation frequency of this circuit is not affected by constituent elements of circuit and the operation is extremely stable. The relationship between the input data and the oscillation frequency is linear. Also, since this circuit is configured to distribute the 1+1/k dividing clock in a cycle of the output signal at constant intervals, the duty ratio of the output signal is always 50%. Furthermore, since this circuit has a perfect digital configuration, miniaturization can be expected at the time of integration.*
Keywords: Digitally controlled oscillator, 1+1/k divider, Multi-phase clock, PLL

1. **Introduction.** There are various types of oscillators, such as a crystal oscillator using a crystal unit, a CR oscillator, an LC oscillator, a multivibrator, and a ring oscillator. Among them, various circuits such as a system using a crystal unit and a multi-vibrator are proposed for an oscillator that generates clock pulses [1,2]. In particular, a voltage-controlled oscillator (VCO) that can control the oscillation frequency by an external voltage is one of the important components in the phase locked loop (PLL) [3]. The PLL can obtain an output signal whose phase and frequency are synchronized with respect to the input signal. This circuit has an important part as a synchronous clock generator in the system of various communication equipment. In recent years, digitization of each system is required against the background of miniaturization, stabilization, and low power consumption. Therefore, on the premise of incorporating the PLL into the system, studies of PLL based on all digital configurations have been made in various fields [4-7].

In all digital PLL, there is a digitally controlled oscillator (DCO) as an oscillator replacing the VCO. DCO is a system that controls its oscillation frequency by using a digital value instead of the external voltage of the VCO. The conventional DCO is realized as an LC oscillator composed by a negative resistance made of MOS, an inductance L and a capacitor C. This DCO digitally changes the electrostatic capacitance of the capacitor C by inputting a control voltage of "0" or "1" to many MOS varactor arrays connected in parallel. For this reason, the internal operation of the conventional DCO will include analog elements. In addition, variations in electrostatic capacitance characteristics of each varactor cause a factor of lowering the accuracy of the oscillation frequency. Also,

DOI: 10.24507/icicelb.09.12.1233

since the conventional DCO contains inductance in its components, it was a bottleneck in making PLL based on all digital configurations into one chip [8].

In this paper, we propose DCO using $1+1/k$ frequency divider based on multi-phase clock. Since the proposed DCO has a perfect digital configuration, its oscillation frequency is not affected by constituent elements etc., so its operation is extremely stable. In addition, miniaturization can be expected at the time of integration. Also, since the output signal has evenly arranged the $1+1/k$ dividing clocks in the one cycle period, its duty ratio is always 50%. In Chapter 2, we describe the circuit configuration of the proposed DCO using $1+1/k$ frequency divider. In Chapter 3, we analyze the operation of the proposed DCO. In Chapter 4, we show the simulation results by Verilog-HDL. Finally, Chapter 5 is a conclusion.

2. DCO Using $1+1/k$ Frequency Divider.

2.1. Circuit configuration of proposed DCO. Figure 1 shows the circuit configuration of the proposed DCO using $1+1/k$ frequency divider based on multi-phase clock. Here, "k" in the $1+1/k$ frequency divider is the multiphase clock number which is the input signal. The divider-$1\sim z$ and selector are frequency dividers and selectors for distributing the $1+1/k$ dividing clock in one cycle of the output signal. The divider-$1\sim z$ are set to $2^1, 2^2, \ldots, 2^z$, respectively. The $1+1/k$ frequency divider divides the multiphase clock by $1+1/k$ only when the clock from the OR gate is low level. The mp-counter and the DC are counters and digital comparators for generating the output signals by counting the $1+1/k$ dividing clock and the normal clock.

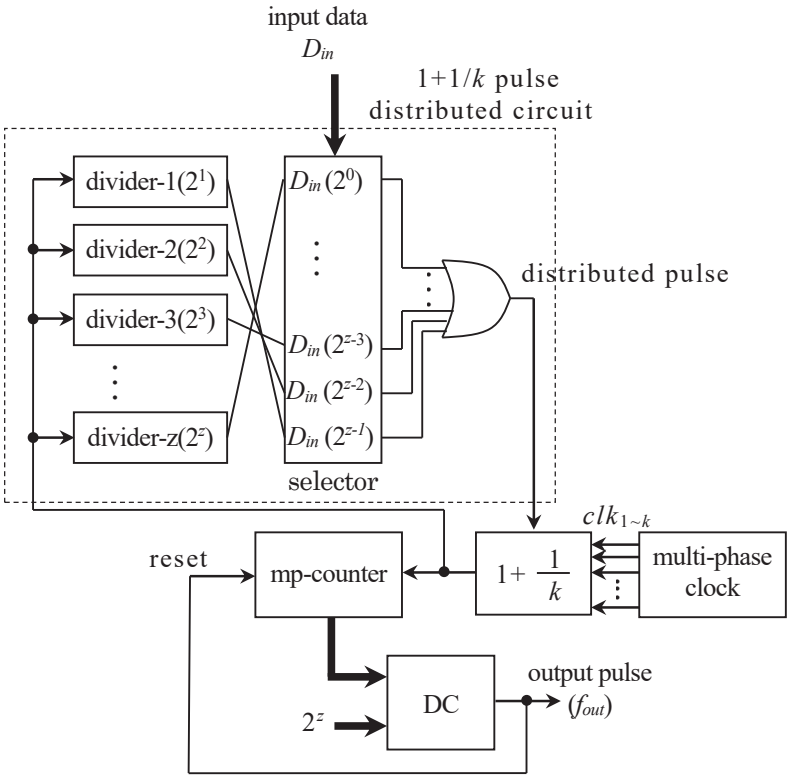
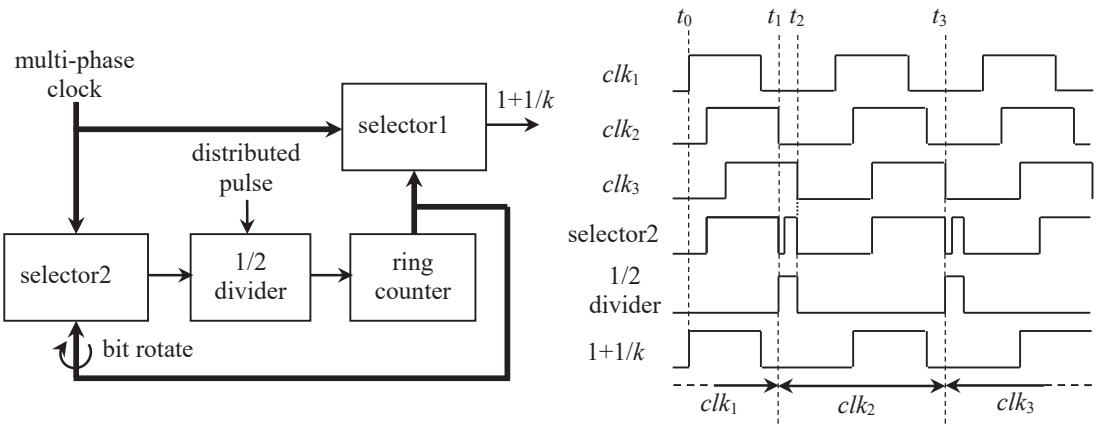


FIGURE 1. Circuit configuration of proposed DCO

2.2. Operation of $1+1/k$ frequency divider. Figure 2 shows the circuit configuration and the operational waveforms of $1+1/k$ frequency divider. This circuit is constructed from two selectors (selector1 and selector2), a 1/2 divider with negative-edge operation, and a ring counter. As shown in Figure 2, for the connection from the ring counter to



(a) 1+1/k divider (b) timing chart

FIGURE 2. Circuit configuration and waveforms of 1+1/k divider

selector2, the connection signal is rotated to the left by one bit and the most significant bit of the ring counter is connected to the least significant bit of selector2. The selector1 and selector2 are connected so that $clk_1, clk_2, \ldots, clk_k$ are selected sequentially from the least significant bit of the selection signal from the ring counter. Also, the bit number of the ring counter is set equal to the multi-phase clock number k.

When the first bit of the ring counter is "1" at time t_0, selector1 selects the multi-phase clock clk_1. Since the second bit is high level in the selection signal of selector2, the multi-phase clock clk_2 is selected. When clk_2 becomes low at time t_1, the output of the 1/2 divider becomes high by the falling edge, and the ring counter is counted up. As a result, the second bit of the ring counter becomes high, so the selector1 outputs clk_2. Simultaneously, selector2 selects multi-phase clock clk_3, and the output of the 1/2 divider becomes low at time t_2. The 1+1/k frequency divider performs a similar operation at time t_3, and outputs clk_3 from selector1. Subsequently, since the same operation is repeated, the 1+1/k frequency divider always selects the next multi-phase clock. Therefore, the time t_{mp} of one period of the output signal is given by

$$t_{mp} = t_d + \frac{t_d}{k} = t_d \left(1 + \frac{1}{k}\right) \tag{1}$$

where t_d is the time of one period of the multi-phase clock. Accordingly, the output frequency f_{mp} of the 1+1/k frequency divider is given by

$$f_{mp} = \frac{f_d}{1 + \dfrac{1}{k}} \tag{2}$$

where f_d is the frequency of the multi-phase clock. From Equation (2), it can be seen that the circuit in Figure 2 operates as a 1+1/k frequency divider.

Also, by applying a distributed pulse shown in Figure 1 to 1/2 divider and stopping its operation when it is at high level, operation of the ring counter of the next stage also stops. Consequently, selector1 and selector2 hold the selected value at that time, so the 1+1/k frequency divider outputs the selected multi-phase clock as it is. In other words, the 1+1/k frequency divider performs frequency division only when the distributed pulse is at the low level.

2.3. **1+1/k dividing clock distributed circuit.** Here, the circuit configuration and operation of the 1+1/k dividing clock distribution circuit will be described. Figure 3 is the operation waveform of the 1+1/k dividing clock distributed circuit when divider-z is

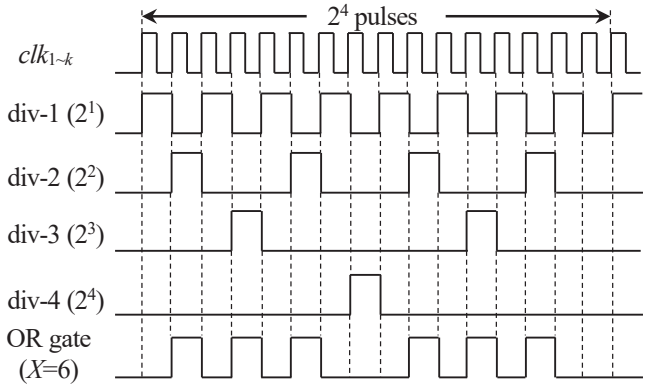


FIGURE 3. Waveforms of $1+1/k$ dividing clock distributed circuit

set to 2^4. In order to set the $1+1/k$ dividing clock to a constant interval in one cycle of the output signal of the DCO, the divider-$1\sim z$ are shifted by one pulse for the input clock and the operation is started. As a result, as shown in Figure 3, the output pulses of the divider-$1\sim z$ do not overlap in time, and a constant interval is maintained for the input clock.

Next, we will explain the extraction of the distributed signal. Each counters (2^1 to 2^z) and the selection signal D_{in} (0 to 2^{z-1}) of the selector sequentially cross and connect from the highest value to the lowest value. From this, for example, when $D_{in} = 6$, $D_{in} = 2^2 + 2^1$, so that pulses from divider-3 (2^3) and divider-2 (2^2) are selected by the selector. The extracted signal controls the $1+1/k$ frequency divider through the OR gate shown in Figure 1. Therefore, the proposed DCO is possible that keeps constant the interval of the $1+1/k$ dividing clock for one cycle of the output signal consisting of 2^z cycles of the multi-phase clock.

When the input data value D_{in} becomes larger than the period 2^z of the multi-phase clock constituting one cycle of the output signal, in order to keep the $1+1/k$ dividing clock at constant intervals, the proposed DCO must further increase the division ratio upper limit value of the divider-$1\sim z$. Therefore, the range of the input data value D_{in} of the proposed DCO is limited to the upper limit value 2^z of divider-$1\sim z$.

3. **Operation Analysis of DCO.** Figure 4 shows the operation waveform of the proposed DCO when divider-$1\sim z$ are set to $2^1\sim 2^6$. When the input data value D_{in} is 20 at time t_0, since this value becomes the selector value in the distributed circuit, the sum of the signals from divider-2 (2^2) and divider-4 (2^4) is taken out through the OR gate. The $1+1/k$ frequency divider of the next stage outputs the multi-phase clock selected by the selector1 shown in Figure 2 as it is while the dispersion signal is generated. At other times, the $1+1/k$ frequency divider divides the multiphase clock by $1+1/k$ by the value (X) minus 64 from $D_{in} = 20$. The mp-counter counts these two signals, and when it reaches 64, the output signal is output from the DC3, and the mp-counter is reset at the same time. After that, since the same operation is repeated, the output of the DCO becomes a signal obtained by dividing only 44 cycles out of 64 cycles of the multi-phase clock by $1+1/k$ frequency divider.

Next, when the input data value D_{in} reaches 40 at time t_1, the output signal becomes a signal obtained by $1+1/k$ dividing only 24 cycles out of 64 cycles of the multi-phase clock from the above operation. Therefore, the oscillation frequency of the DCO becomes higher than that when the input data value D_{in} is 20, so it is found that the oscillation frequency can be controlled according to D_{in}.

Here, we consider the oscillation frequency of the proposed DCO. The proposed DCO is configured to control the oscillation frequency by changing the number of $1+1/k$ division

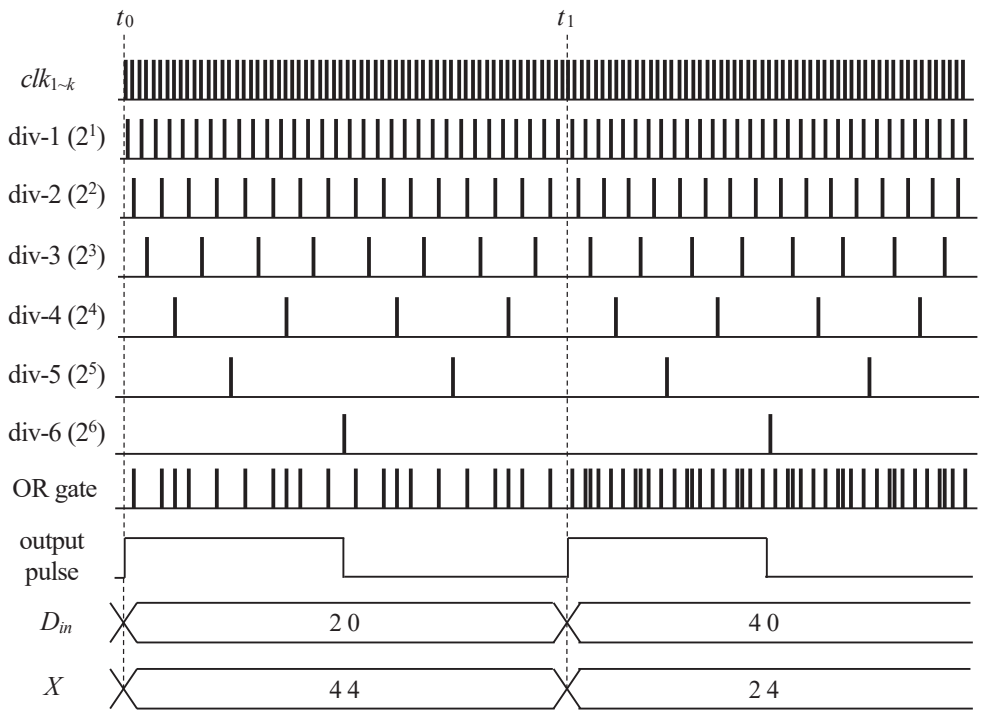


FIGURE 4. Waveforms of proposed DCO

in one cycle of the output signal according to the input data value D_{in}. The relation between the input data value D_{in} and the $1+1/k$ dividing number X becomes "n" decrease/increase of X for "n" increase/decrease of D_{in}. Therefore, from Equations (1) and (2), the oscillation frequency f_{out} of the proposed DCO is expressed by

$$f_{out} = \frac{1}{t_{mp}\left(2^z - D_{in}\right) + t_d \cdot D_{in}} = \frac{1}{t_d\left[\left(1+\frac{1}{k}\right)\left(2^z - D_{in}\right) + D_{in}\right]}$$
$$= \frac{f_d}{\left(1+\frac{1}{k}\right)\left(2^z - D_{in}\right) + D_{in}} \tag{3}$$

Next, we consider the oscillation frequency range of the proposed DCO. Since the minimum value of the input data value D_{in} is "0" and the maximum value is 2^{z-1} from Section 2.3, from Equation (3), the oscillation frequency range is given by

$$\frac{f_d}{\left(1+\frac{1}{k}\right)2^z} \sim \frac{f_d}{\left(1+\frac{1}{k}\right)} \quad \left(2^z \geq D_{in}\right) \tag{4}$$

Therefore, in order to expand the frequency range of the proposed DCO, it is necessary to set "z" large or set f_d high. In addition, from Equation (4), the free running frequency f_{fr} of the proposed DCO in the state where the input data value D_{in} is not input is expressed by

$$f_{fr} = \frac{f_d}{\left(1+\frac{1}{k}\right)2^z} \tag{5}$$

Next, we consider the time resolution of the proposed DCO. The proposed DCO controls the oscillation frequency by increasing/decreasing the number of $1+1/k$ dividing clock in one cycle of the output signal. Since the increment/decrement unit of $1+1/k$ dividing

number is "1", the oscillation frequency is controlled by the time unit of the phase interval of the multi-phase clock. Therefore, the time resolution Δt_{out} of the proposed DCO is expressed by

$$\Delta t_{out} = \frac{t_d}{k} \tag{6}$$

From this, it is found that in order to realize the operation of approximation to the analog VCO by setting the time resolution high, it is sufficient to increase the multi-phase clock number k. However, since k and the oscillation frequency range are in the relation between contraries from Equation (4), it is necessary to consider the application in designing.

4. **Simulation Results.** This simulation was described using Verilog-HDL as hardware description language. In this simulation, the upper limit of the count value of divider-1$\sim z$, the number and frequency of multi-phase clock are set to $2^z = 2^6$, $k = 7$ and $f_d = 7$MHz, respectively.

Figure 5 shows the simulation waveform of the proposed DCO when the input data value is set to 40. From this, in the proposed DCO, the selector retrieves divider-1 (2^1) and divider-3 (2^3). Therefore, in the proposed DCO, 40 cycles are divided by $1+1/k$ with respect to the output signal composed of multi-phase clock of 64 cycles, and the interval is constant.

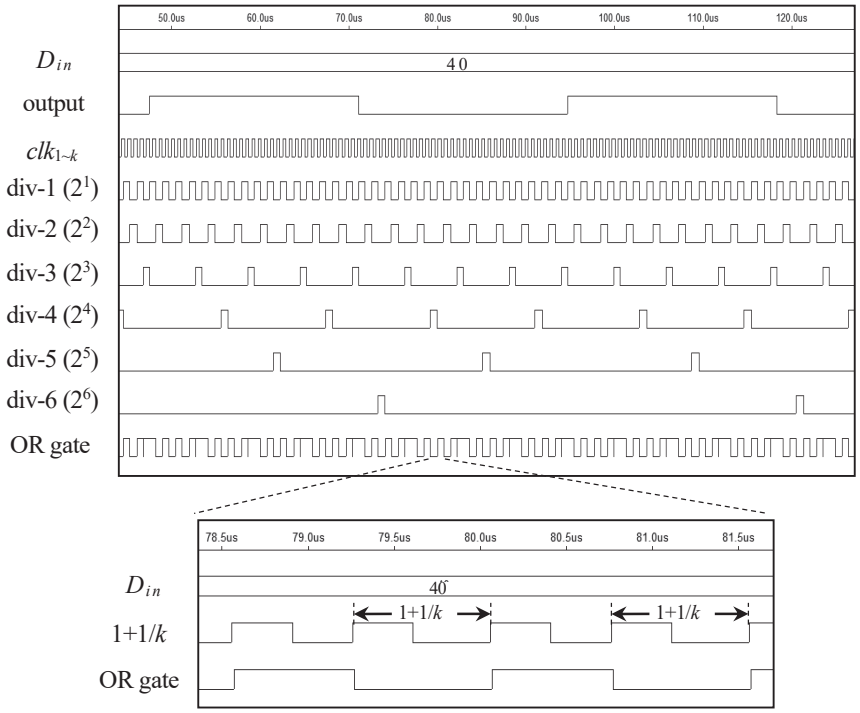


FIGURE 5. Simulation waveforms of proposed DCO

Figure 6 is the simulation waveform of the proposed DCO in the step response when the input data is changed between 10 and 40. From this, since the oscillation frequency changes according to the change of the input data, it is found that the proposed DCO can obtain the expected operation for the step response.

Figure 7 shows the relationship between the input data D_{in} and the oscillation frequency f_{out} of the proposed DCO based on the same setting as above. From this, it is found that the relationship between D_{in} and f_{out} shows linearity and operates within the range satisfying Equations (3) and (4). In addition, it is also found that the time resolution changes at $\Delta t_{out} = 20$ns and satisfies Equation (6).

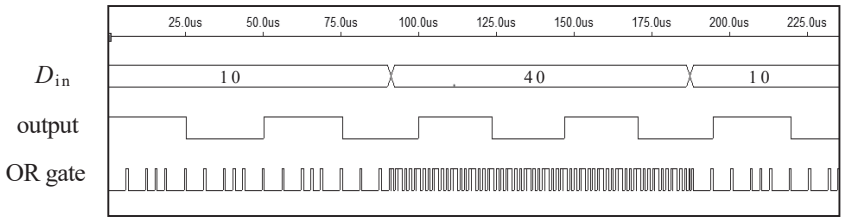


FIGURE 6. Simulation waveforms for step response

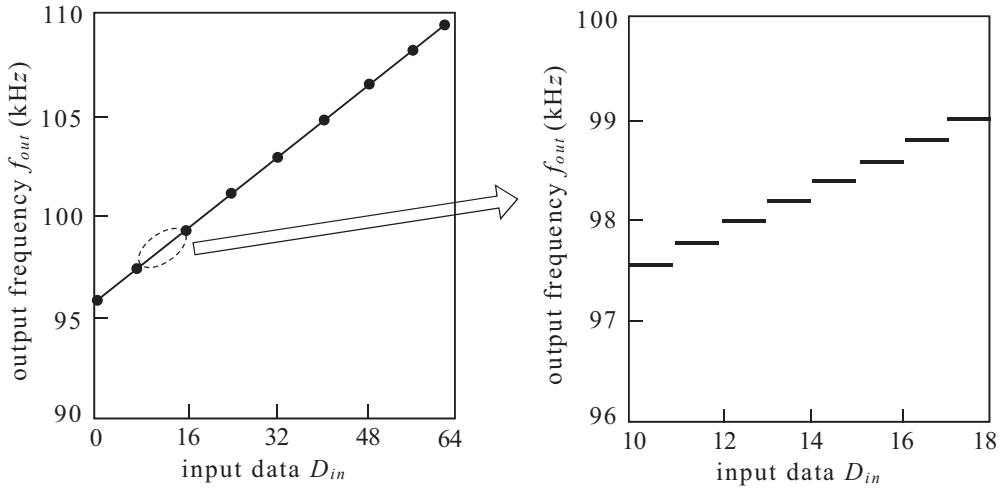


FIGURE 7. Relationship between input data D_{in} and oscillation frequency f_{out}

5. **Conclusion.** In this paper, we proposed the digitally controlled oscillator based on multi-phase clock with an all digital configuration which improved the conventional problems. Since this circuit has a perfect digital configuration, miniaturization can be expected at the time of integration. The oscillation frequency is not affected by constituent elements of circuit and the operation is extremely stable. Also, the relationship between the input data and the oscillation frequency is linear. Furthermore, since this circuit is configured to distribute the $1+1/k$ dividing clock in a cycle of the output signal at constant intervals, the duty ratio of the output signal is always 50%.

In recent years, systems that perform signal processing using both rising and falling edges of a clock signal are increasing. Therefore, by utilizing the proposed DCO having the above characteristics for all digital PLLs, it can be expected to be used for clock supply sources etc. in various digital communication equipment systems supporting future IoT.

In the future, we plan to extend the oscillation frequency operation range of the proposed DCO and verify the characteristics when it is applied to all digital PLL.

REFERENCES

[1] T. Shiono, S. Kubo, M. Ito, Y. Shimizu and K. Tuchikura, The frequency adjustment method of the quartz crystal unit using quick response evaporation source, *IEICE Trans. Electronics*, vol.J89-C, no.4, pp.137-144, 2006.

[2] H. Sasaki, H. Isoguchi, A. Julsereewong, P. Julsereewong, M. Yahara and H. Sasaki, Low voltage and self-statable differential type astable multivibrator using CMOS-XOR/XNOR gates, *IEICE Trans. Electronics*, vol.J95-C, no.5, pp.101-104, 2012.

[3] M. Nakamura, A. Yamagishi and M. Harada, A voltage-controlled oscillator using a MOS transmission gate to reduce bias noise, *IEICE Trans. Electronics*, vol.J89-C, no.10, pp.663-665, 2006.

[4] F. Sato, T. Saba, D. Park and S. Mori, Digital phase-locked loop with a wide locking range using fractional divider, *IEICE Trans. Communications*, vol.J78-B-I, no.1, pp.86-93, 1995.

[5] K. Fujimoto, H. Sasaki and M. Yahara, A dividing ratio changeable digital PLL with low jitter using a multiphase clock divider, *IEEJ Trans. Electronics, Information and Systems*, vol.129, no.3, pp.399-405, 2009.

[6] H. Sasaki, M. Yahara, K. Fujimoto and H. Sasaki, A fractional multiplier by phase locked loop using multi-phase clock divider, *ICIC Express Letters*, vol.7, no.4, pp.1183-1188, 2013.

[7] Y. Harada, M. Yahara, K. Matsumoto and K. Fujimoto, A programmable divider with 50% duty cycle unrelated to dividing cycle and its application to PLL, *IEEJ Trans. Electronics, Information and Systems*, vol.135, no.1, pp.2-7, 2016.

[8] M. Elkholy and K. Entesari, A wideband low-power LC-DCO-based complex dielectric spectroscopy system in 0.18-μm CMOS, *IEEE Trans. Microwave Theory and Techniques*, vol.65, no.11, pp.4461-4473, 2017.