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A 2-MODE DIGITAL FLL USING FREQUENCY COMPARATOR CORRESPONDING TO CYCLE SLIP

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Abstract. *For clock generators used inside portable information devices, it is desirable to quickly restart to a stop state from the viewpoint of low power consumption. In this paper, we propose a 2-mode FLL (Frequency-Locked Loop) with all digital configuration. In this circuit, by using the fast frequency pull-in circuit, not only the pull-in time is 1 period of the input signal, but also the phase of input and output signals agrees. Also, it is possible to obtain the output signal with extremely accurate frequency and the wide frequency lock-in range for input signal. Moreover, the frequency comparator using in this FLL also corresponds to the cycle slip between input and output signals, so that the stable output signal with low jitter can be obtained.*
Keywords: FLL, Cycle slip, Frequency comparator, Fast pull-in, PLL

1. **Introduction.** In mobile information devices driven by batteries, it is desirable to operate with the low power consumption from the viewpoint of battery life. In particular, in the use of portable information equipment, since the period in which a system is in standby state is extremely long, the power consumption in this state greatly affects the reduction of power consumption of entire system. In order to reduce the power consumption, the supply of clock signal to the system is greatly concerned. Therefore, if the clock generator is stopped during the standby state, not only the supply of clock signal to the system can be stopped, but also the power consumption related to the clock generator can be reduced [1]. However, when the system returns from the standby state, the quick supply of clock signal becomes a very important matter which affects the performance of entire system.

One of the circuits widely used as a clock generator is a PLL (Phase-Locked Loop). PLL is the circuit that outputs the signal locking frequency and phase for the input signal. This circuit is used in a wide range of fields such as a frequency synthesizer, a demodulation of various signals, and a rotation control of the motor. However, PLL requires the lock of frequency and phase until the output clock is generated after adding the input signal, so that it is required a long time to generate the stable output clock. For this reason, since PLL cannot expect to the return from stopping state at short time, it is difficult to stop the operation of PLL during the system in standby state. As a result, the use of PLL has difficulty in suppressing the power consumption of system at standby time [2-4].

On the other hand, there is FLL (Frequency-Locked Loop) as a circuit for generating a clock in which only the frequency is locked for input signal. FLL is not locked the phase

between input and output signals, so that the time to obtain the stable output clock after adding input signal can be greatly shortened as compared with PLL. Therefore, in a system that does not require the phase lock, since FLL is possible to stop the operation during standby state, it is extremely advantageous compared with PLL from the viewpoint of power consumption. Also, the phase of FLL is not locked, so it is not affected by the clock propagation delay in system and the discontinuous points in the phase of input signal [5,6].

However, in the conventional FLL, it is difficult to construct the frequency comparator which detects the frequency error between input and output signals accurately and quickly, so that there is a problem that the frequency precision of output signal is low. Therefore, although FLL is advantageous compared to PLL, it is not used much in current systems.

In this paper, we propose a 2-mode DFLL (Digital FLL) that realizes the output signal with extremely accurate frequency and the fast frequency pull-in [7,8]. In the proposed DFLL, since the frequency error of output signal for the input signal is less than 1 pulse width of the reference clock, it can be obtained the extremely accurate output signal. In addition, by constructing the 2-mode DFLL that operates the fast pull-in circuit at time of startup, the frequency pull-in can be finished in 1 period of the input signal. Moreover, this circuit can obtain the stable output signal with low jitter without being affected by the cycle slip between input and output signals.

Below, in Chapter 2, we analyze the circuit configuration of the proposed 2-mode FLL and its operation. In Chapter 3, we describe the relationship between frequency lock-in range and steady frequency error. In Chapter 4, we show simulation results by Verilog-HDL. Finally, Chapter 5 is a conclusion.

2. **Proposed 2-Mode DFLL.**

2.1. **Block configuration.** Figure 1 shows the circuit configuration of the proposed 2-mode DFLL. Here, FC is a digital frequency comparator corresponding to the cycle slip. FC outputs not only a digital value for the frequency error between input and output signals but also a lead or lag signal of the phase. FER is an adjustment circuit for removing the frequency error between input and output signals calculated by FC. Divider is a variable frequency divider that divides the reference clock according to the output value of FER and generates the output signal. FFP is a fast frequency pull-in circuit that

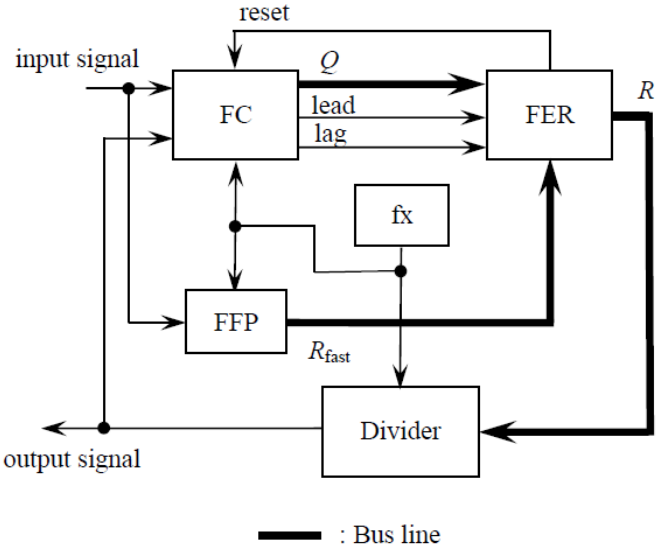

FIGURE 1. Block diagram of the proposed DFLL

realizes the 2-mode operation by improving the pull-in characteristic at time when the input signal is added. fx is the reference clock source for controlling the loop.

2.2. **Frequency comparator.**

2.2.1. *Conventional frequency comparator.* First, the frequency comparator used in conventional FLL will be described. As conventional frequency comparator, there is a system using a monostable multivibrator, a flip-flop, and a constant current source.

The frequency comparator using two monostable multivibrators operates each circuit setting the same time constant at each rising edge of input and output signals. And the frequency error between input and output signals is detected by comparing the average value of respective output pulses. In this method, there is a problem that the error of time constant of two monostable multivibrators and the accuracy of pulse width detection circuit directly lead to the frequency error.

The frequency comparator using flip-flop is configured to detect the frequency error by using the pulse width generated when the cycle slip occurs between input and output signals. In this system, the frequency error can be detected relatively accurately as compared with the method using monostable multivibrator. However, since this circuit can obtain the frequency error only when the cycle slip occurs, there is a problem that the output jitter of loop increases.

The frequency comparator using constant current source can detect the frequency error even if the cycle slip between input and output signals does not occur, so that the output jitter of loop can be suppressed as compared with above two systems. Also, since each component element is one, it is not affected by the relative error due to elements as compared with the frequency comparator using monostable multivibrator. However, this system is restricted to suppress the output jitter of loop, because it can obtain the frequency error only every 4 periods of input signal. Further, since this system is constituted by a FET switch, a capacitor, and an operational amplifier, there is a problem that it is difficult to use in a high frequency region.

2.2.2. *Circuit configuration and operation of proposed digital frequency comparator.* Figure 2 shows the circuit configuration of the proposed digital frequency comparator corresponding to the cycle slip. In this circuit, the pulse at point O corresponding to the frequency error is configured to be inverted at rising edge of either the input signals A or B (output signal of DFLL). The reason for this is to detect an appropriate frequency error even when the cycle slip occurs between the input signals A and B.

Next, we explain circuit operation. Figure 3 shows the operating waveforms of the proposed digital frequency comparator. At time t_1, when the input signal A rises up, the point O in Figure 2 becomes high level. Next, when the input signal B rises up at time

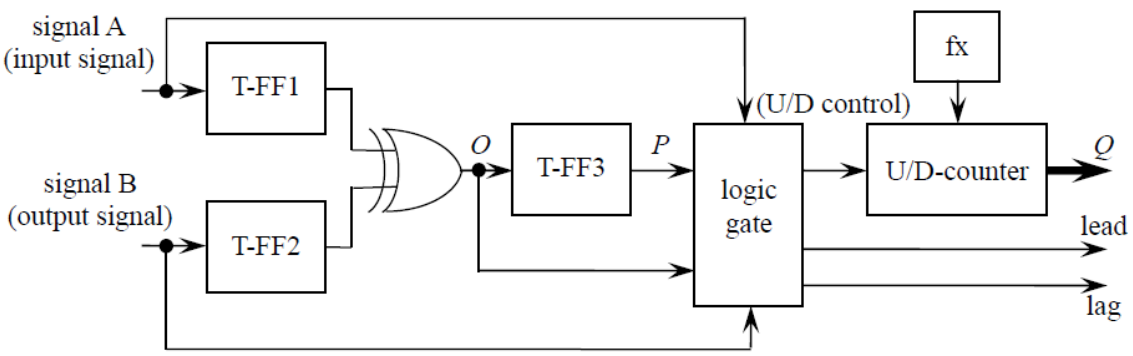

FIGURE 2. Circuit configuration of the proposed digital frequency comparator

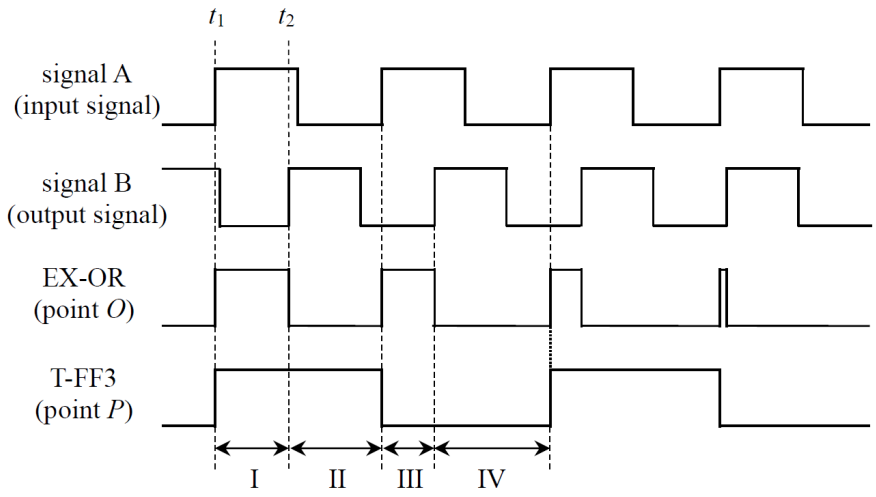

FIGURE 3. Waveforms of the proposed digital frequency comparator

t_2, the point O becomes the low level. This pulse at point O is divided by T-FF3. (Point P)

Next, we explain the detection operation of frequency error. In the state I of Figure 3, U/D-counter up-counts the reference clock number that passes while the point O is at the high level, from the initial value "X". Assuming that the reference clock number (up-count value) passes while the state I is "Y", the count value "Q" of U/D-counter is "$X+Y$" at the end of state I.

In the state II, the count value "Q" is held.

In the state III, U/D-counter down-counts the reference clock number that passes while the point O is at the high level. Assuming that the reference clock number (down-count value) passes while the state III is "Z", the count value "Q" is "$X+Y-Z$". As a result, the count value "Q" becomes a value corresponding to the frequency error between input signals A and B at the end of state III.

In the state IV, the count value "Q" is transferred to FER of the next stage. If the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y > Z$", FER decreases the output value which becomes the dividing ratio "R" of Divider by the value corresponding to the frequency error. When the dividing ratio before state IV is "R_{pre}", the dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} - (Y - Z) \tag{1}$$

As a result, the output frequency of the proposed DFLL increases according to the difference between "Y" and "Z", so that it operates to remove the frequency error between input and output signals.

Conversely, if the up-count value "Y" and the down-count value "Z" satisfy the relation of "$Y < Z$", FER increases the output value by the value corresponding to the frequency error. The dividing ratio "R" at this time becomes as follows.

$$R = R_{pre} + (Z - Y) \tag{2}$$

As a result, the output frequency of the proposed DFLL decreases according to the difference between "Y" and "Z", so that it performs the same removing operation. Also, the count value "Q" of U/D-counter is set to the initial value "X" for the next count at this time.

In addition to this, the dividing ratio "R" is controlled as shown in Table 1 according to the phase lead or lag states between input and output signals.

TABLE 1. Control state of dividing ratio according to the phase lead or lag

	state I	state III	Equation (1)	Equation (2)
Pattern 1	lead	lead	$R = R_{pre} - (Y - Z)$	$R = R_{pre} + (Z - Y)$
Pattern 2	lead	lag	$R = R_{pre} + (Y - Z)$	$R = R_{pre} + (Z - Y)$
Pattern 3	lag	lead	$R = R_{pre} - (Y - Z)$	$R = R_{pre} - (Z - Y)$
Pattern 4	lag	lag	$R = R_{pre} + (Y - Z)$	$R = R_{pre} - (Z - Y)$

2.2.3. *Response to cycle slip.* Here, we consider the cycle slip problem. Figure 4 shows the operating waveforms of the proposed frequency comparator and the conventional frequency error detection by RS-FF in the case where the cycle slip occurs between input and output signals.

First, we describe the cycle slip problem of the conventional frequency error detection by RS-FF. In the conventional comparator, the frequency error detection pulse becomes high level at the rising edge of input signal A and low level at the rising edge of input signal B. Therefore, from time t_1 to t_2, it is possible to output an appropriate detection pulse according to the frequency error between input and output signals. However, when the cycle slip occurs at time t_3, the detection pulse becomes high level from time t_4 to t_5, so that it cannot detect the appropriate frequency error.

On the other hand, the proposed frequency comparator is configured to invert the detection pulse at the rising edge of either input signals A or B. Therefore, from time t_1 to t_2, the detection pulse is the same as the conventional circuit. When the cycle slip occurs at time t_3, the proposed frequency comparator inverts the detection pulse at the rising edge of input signal B (time t_4) and performs the appropriate error detection. Consequently, this comparator can always detect the appropriate frequency error without being affected by the cycle slip.

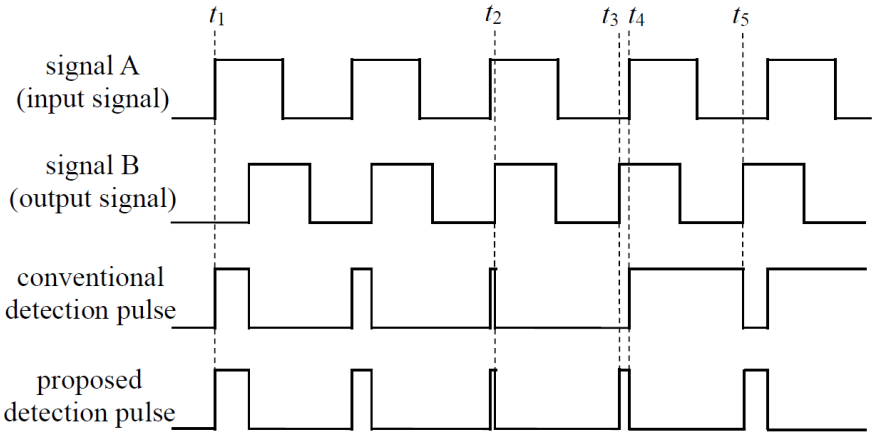

FIGURE 4. Waveforms of the conventional type and the proposed frequency comparator at occurrence of cycle slip

2.3. **2-mode operation.** The frequency locked time after start-up DFLL is shorter than that of PLL because it is not necessary for the phase lock, but the several periods of input signal are required. However, in consideration of the low power consumption in portable information equipment, a faster frequency locked state from the system standby is desired.

Figure 5 shows the process of the frequency pull-in in the proposed 2-mode DFLL. When the first input signal is added at time t_1, FFP shown in Figure 1 counts the reference clocks number "R_{fast}" that passes while 1 period of the input signal up to time t_2. Next, at the

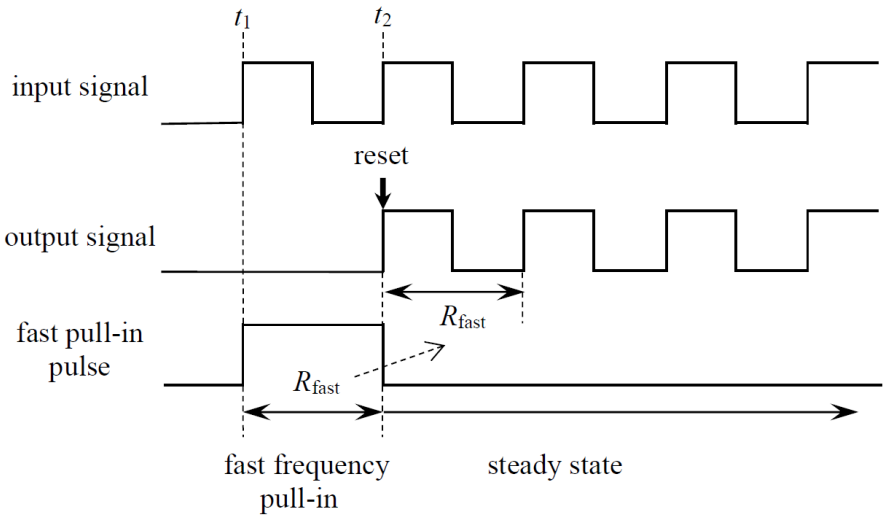

FIGURE 5. Process of the frequency pull-in in the proposed 2-mode DFLL

rising edge of second period of the input signal (time t_2), this count value "R_{fast}" is set to FER which determines the dividing ratio of Divider. As a result, the proposed 2-mode DFLL can obtain the output signal that the frequency locked from the second period of input signal. In addition, since this DFLL is reset at the rising edge of second period of the input signal, the phases of input and output signals are matched. Therefore, by using the 2-mode DFLL, it is also possible to distribute signals that the phases are locked with the internal clock to each system as the clock distribution circuit.

3. **Frequency Lock-in Range and Steady Frequency Error.** The proposed DFLL is configured to determine the frequency of output signal by dividing the reference clock fx with the dividing ratio "R". Therefore, the frequency lock-in range is determined by the setting range of "R".

Here, when the lower limit value of the dividing ratio is "$R_{\min}$" and the upper limit value is "$R_{\max}$", the frequency lock-in range of the proposed DFLL is determined as follows.

$$\frac{f_s}{R_{\max}} \geq f_{in} \geq \frac{f_s}{R_{\min}} \tag{3}$$

where f_{in} is the frequency of input signal and f_s is the frequency of the reference clock.

Next, we consider the frequency error in the steady state. Figure 6 shows the relationship between reference clock and input signal in the steady state. The reference clock and the input signal are not locked. Therefore, in the steady state, as shown between time t_1 and t_2 in Figure 6, a time difference occurs between the rising edge of reference clock and the input signal. This time difference is less than 1 period of the reference clock at maximum. The output signal of the proposed DFLL is determined by dividing the reference clock. That is, in the steady state, this DFLL has a steady frequency error of less than 1 period of the reference clock at the maximum. However, the error occurring in 1 period of the input signal is within 1 pulse width of the reference clock. Therefore, if the dividing ratio "R" is set to a certain large value, the influence on the jitter suppression effect by this error is considered to be negligible. The average frequency f_{avg} of the output signal is expressed as follows.

$$f_{avg} = \frac{\left(\frac{1}{R} + \frac{1}{R \pm 1}\right)}{2} f_s \tag{4}$$

In this way, the output frequency changes in accordance with the input frequency, and the frequency lock is continued.

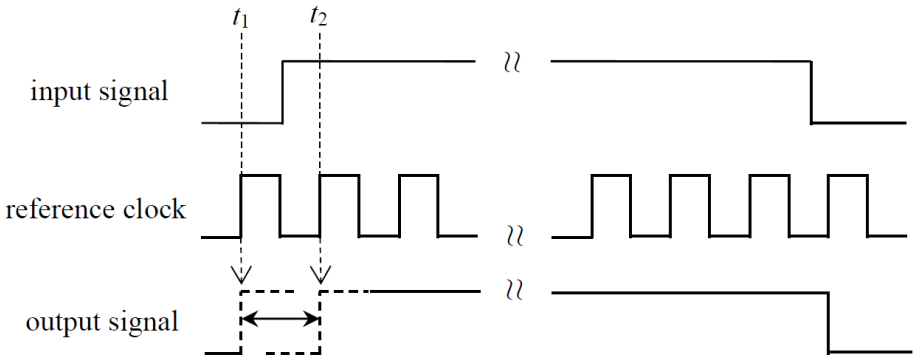

FIGURE 6. Relationship between the reference clock and the input signal in steady state

4. **Simulation Results.** This simulation was described using Verilog-HDL as hardware description language.

Figure 7 shows the simulation waveforms of each part of the proposed DFLL in the steady state. From this, it is found that the dividing ratio "R" that determines the frequency of output signal operates within the range satisfying Equation (4).

Figure 8 shows the simulation waveform of each part at the 2-mode operation in the proposed DFLL. From this, it is found that the frequency lock is finished 1 period after the input signal is added. It is also found that the phases of input and output signals are in agreement after the frequency lock.

In addition, we confirmed by simulation that the frequency lock-in range of the proposed DFLL satisfies Equation (3).

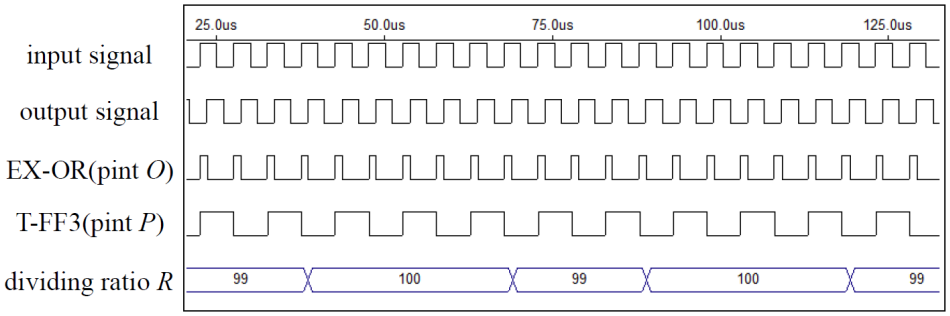

FIGURE 7. Simulation result of the proposed DFLL

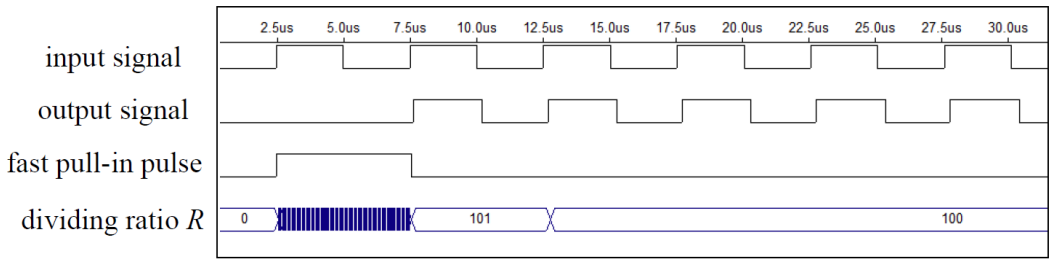

FIGURE 8. Simulation result of the fast frequency pull-in at 2-mode operation

5. **Conclusion.** In this paper, we proposed the 2-mode DFLL with all digital configuration. In this circuit, since the frequency error in the steady state is less than 1 pulse width of the reference clock, it is possible to obtain the frequency of output signal with high accuracy for the input signal. Also, the frequency lock-in range is extremely wide. By using the fast frequency pull-in circuit, the pull-in time of this circuit is 1 period of the input signal, and the phase of the output signal agrees with that of the input signal. Furthermore, this circuit can obtain the stable output signal with the low output jitter without being affected by the cycle slip between input and output signals.

In the future, we will consider the further reduction of the steady frequency error and the problem of pseudo-lock in which the frequency of input and output signals are locked in relation other than the set value.

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