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A DIGITAL FAST CORRECTOR POWER CONVERTER DESIGN FOR TPS RING

Yuanchen Chien, Chenyao Liu and Baosheng Wang

Department of Power Supply Group
National Synchrotron Radiation Research Center
No. 101, Hsin Ann Road, Hsinchu 300, Taiwan
wang.bs@nsrrc.org.tw

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Abstract. *In the beginning of 2016, TPS (Taiwan Photon Source) has started its light source services to users. TPS, a 3rd generation synchrotron light source, is newly constructed to provide high brightness beam source for a variety of scientific researchers. To maintain the electronic beam orbit stability, fast orbit feedback system (FOFB) is essential to suppress the unwanted disturbances from different noise sources. The FOFB system is composed of fast corrector magnets, wide bandwidth power supplies, beam position data and orbit compensation algorithm to serve the noise suppression purpose. It is shown that FOFB system is effective in stabilizing the beam position. This paper describes a new type full-digital corrector power supply to serve as the driving source to feed the fast corrector magnet in the FOFB system, where both wide bandwidth and fast transient response are needed. The new power supply employs the same power stage of the analog fast corrector power supply, and the current output regulation is redesigned and implemented in NI-sbRIO9606, which embeds a real-time processor and a user-reconfigurable FPGA (Field Programmable Gate Array) on a single module from National Instruments. The simulation and prototype result indicates that the new power supply can deliver operational bandwidth at about 10 KHz and faster transient behavior compared to the along version of the fast corrector power supply.*

Keywords: Synchrotron, Fast corrector, Wide bandwidth, Embedded controller, Power supply

1. **Introduction.** TPS is a 3 GeV synchrotron facility with very low emittance and thus is capable of generating ultra-brightness beam source for advanced scientific studies in a variety of areas such as molecular, material, life and medicine related subjects [1]. TPS is a concentric ring, in which booster and storage ring are built and located in the same tunnel. The 50 MeV electron beam coming out of the linear accelerator is ramped up to 3 GeV with 3 Hz repetition rate in the booster ring and then extracted to the storage ring which has a circumference of 518.4 m. The lattice of the TPS storage ring is composed of 24 double-bend cells with 6-fold symmetry. TPS had started commissioning since 2014. It has successfully delivered over 500 mA at the end of 2015 and is scheduled to be ready for user operation in 2016.

For it is designed to have very small beam sizes both in the vertical and horizontal plane, it is required that the beam position stability is in the order of tens of μm. In order to achieve this strict beam position requirement and keep the beam travelling in the defined closed orbit range, fast orbit feedback system (FOFB) has to be utilized [2].

Starting from 2016, the FOFB system is installed, tested and proved to be effective in maintaining the beam trajectory to the reference closed orbit by eliminating perturbations coming from different sources like magnet strength errors, alignment errors and vibration caused by water pipes close to the magnets and other sources [3]. FOFB mainly consists of 3 major key components: beam position monitor (BPM), orbit compensation computation

unit and corrector power supply with specialized fast and slow setting control interface. In FOFB, total 170 BPMs and 96 fast correctors (Horizontal and Vertical Combined Type) are installed in the storage ring lattice; therefore, 192 fast corrector power supplies are needed to provide kick strength to correct the beam position deviation when necessary.

At the present time, bipolar four-quadrant power converter modules with centralized corrector power supply controller (CPSC) are used. There are total 8 power modules each with independent analog PID controller and one CPSC placed in the middle of a racket. The digital current commands are fed from the FOFB system to CPSC, where these commands are translated to analog ones by high-resolution DACs (Digital-to-Analog Converter). The power module is able to deliver 10 A with -3 dB bandwidth up to 3 KHz.

The FOFB system modifies the fast correctors with 10 KHz update rate. The maximum corrected current value is set at 1% of the 10 A output, which is equivalent to maximum 0.1 A per 100 μs (10 KHz). This means that for a maximum 0.1 A step correction, the rise time and settling time of the fast corrector power supply should fall within 100 μs period.

Even these power modules work with the FOFB system currently, common problems associated the analog PID controller still exist. First, it is not easy to realize high-resolution DACs with ultra-low noise. Second, tuning the PID control parameters for all the 192 power supplies is difficult considering the capacitor and resistor value tolerance and component variation of the precision amplifiers used to constitute the analog PID controller. Moreover, the rise and settling time of the step response does not meet the FOFB specifications and the working bandwidth is expected to be wider to further extend FOFB's position error suppression ability to cope with higher frequency beam position perturbation.

This paper describes the design and implementation of a fast corrector power supply with digital control loop based on embedded microprocessor, the virtual software control interface and FPGA [4-6]. With the digital architecture, the time and frequency domain response for 192 power modules is expected to be much more consistent, the PID parameters are easier to adjust and besides these, the working bandwidth is extended and the rise time is reduced with proper controller design and switching scheme strategy. A prototype was also built to verify if its performances meet the desired requests.

The digital fast corrector power converter is capable of delivering ± 10 A at ± 50 V. First, the prototype design is described. Second, the discrete PID controller design is introduced. Third, the hardware implementation is described. At last, the experimental results are presented.

2. **Prototype Design.**

The prototype design is based on the fast corrector power converter module with analog PI control. The corrector power module is developed and constructed by the NSRRC's power supply group of NSRRC and the Center for Measurement Standards of Industrial Technology Research Institute (CMS, ITRI) [7].

The ± 10 A/± 50 V corrector magnet power converter adopts H-bridge topology with 30 KHz switching frequency. MOSFETs with reduced R_{ds} (MOSFET ON resistance) and precision shunt resistor with ultra-low temperature drift and fast frequency response are used to increase the working bandwidth. As a result, the achievable -3 dB bandwidth is 3.4 KHz and rise time of the small signal step response (0.1 A step) is about 142 μs. However, the time domain performance of the analog fast corrector power supply still does not fully satisfy the needs for the FOFB system with 10 KHz update rate, which requires the rise time small signal step response to fall with 100 μs (10 KHz update rate). Hence, in order to speed up the step transient performance and further extend the working bandwidth for better orbit deviation elimination, the controller part of the present fast corrector power module is redesigned in the digital domain.

2.1. **Power circuit topology.** The equivalent circuit topology of the fast corrector power converter is shown in Figure 1. The 48 V DC comes from off-the-shelf 1.5 KW AC-to-DC switching regulator and is connected to the DC bus terminals. The circuit is composed of a filter and energy storage capacitor, four MOSFET switches forming the H-bridge in two legs (S_1/S_3 and S_2/S_4) with embedded anti-parallel diode and damped output low pass filter.

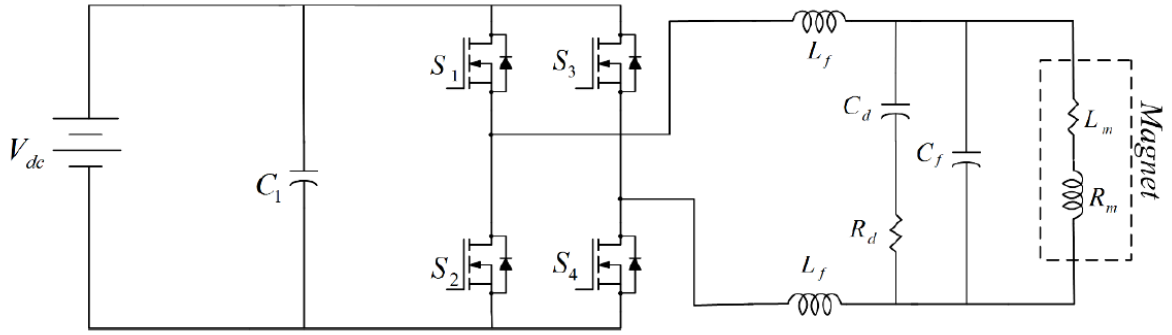

FIGURE 1. Power stage of fast corrector power supply

The design parameters are listed in Table 1.

TABLE 1. Digital fast corrector power supply parameters

TPS Fast Corrector Output Specifications	
Maximum Current Output	±10 A
Maximum Voltage Output	±50 V
Low-pass Filter Parameters	
L_f	100 μH
C_f	0.82 μF
C_d	33 μF
R_d	10 Ohm
Fast Corrector Magnet Parameters	
L_m	2.92 mF
R_m	8.8 mOhm

The s-domain transfer functions of the magnet load $G_L(s)$ and the low pass filter $G_{LPF}(s)$ are expressed as follows:

$$G_L(s) = \frac{1}{R_m + L_m s} \tag{1}$$

$$G_{LPF}(s) = \frac{1 + C_d R_d s}{1 + C_d R_d s + (L_f C_f + L_f C_d)s^2 + R_d C_f C_d L_f s^3} \tag{2}$$

2.2. **Switching methodology.** Complementary unipolar switching scheme is adopted for the pulse-width-modulation (PWM) switching and the switching mechanism is shown in Figure 2 [8]. With this control technique, the MOSFETs of each leg are controlled independently of the other leg and the PWM control signals in the same leg are complement to each other. The switching signals are such that S_1, S_2, S_3 and S_4 are generated by comparing the current command $V_c(t)$ and its negation $-V_c(t)$ to the reference triangular waveform $V_{tri}(t)$. When $V_c(t)$ is greater than $V_{tri}(t)$, S_1 is turned ON, and when $-V_c(t)$ is greater than $V_{tri}(t)$, S_3 is ON, while S_2 and S_4 are complement to S_1 and S_3 respectively. The major benefit with this control scheme is that ripple frequency of the output current I_o will be 100 KHz, which is twice that of the 50 KHz PWM frequency

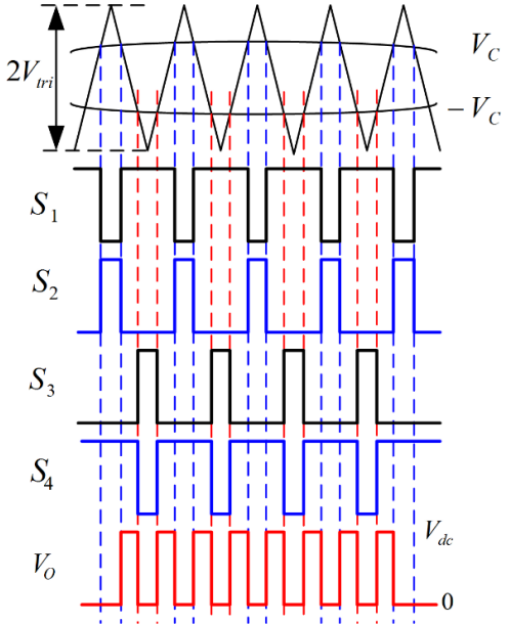

FIGURE 2. Unipolar switching diagram of PWM

and thus, the damped filter design is made easier while the filter component size can be reduced due to this ripple frequency doubling. The transfer function of the PWM scheme can be obtained as follows: Assume that during a switching period T_s, the control input $V_c(t)$ remains constant.

The relation of the on-duty ratio d_{on} and the PWM control input V_c can be approximated and expressed as

$$d_{on} = \frac{1}{2}\left(1 + \frac{V_c}{V_{tri}}\right) \tag{3}$$

$$d_{off} = 1 - d_{on} \tag{4}$$

where V_{tri} is half of the peak-to-peak amplitude of the PWM triangle waveform. And the averaged output voltage V_o is given by

$$V_o = d_{on}V_{dc} - d_{off}V_{dc} \tag{5}$$

By replacing d_{off} in Equation (4) into Equation (5), V_o becomes

$$V_o = (2d_{on} - 1)V_{dc} \tag{6}$$

Then substituting the d_{on} of Equation (3) into Equation (6),

$$k = \frac{V_o}{V_c} = \frac{V_{dc}}{V_{tri}} \tag{7}$$

where k is the derived transfer function of the complementary unipolar switching scheme.

3. **Discrete PID Controller Design.** The overall closed-loop control system can be constructed by using derived transfer functions of the magnet load $G_L(s)$, the low pass filter $G_{LPF}(s)$ and the PWM converter gain k obtained above. The block diagram of the closed loop system is depicted in Figure 3.

The open loop transfer function $T_{open}(s)$ is expressed as

$$T_{open}(s) = \frac{I_e(s)}{I_o(s)} = G_{PID}(s) \cdot k \cdot G_{LPF}(s) \cdot G_L(s) \tag{8}$$

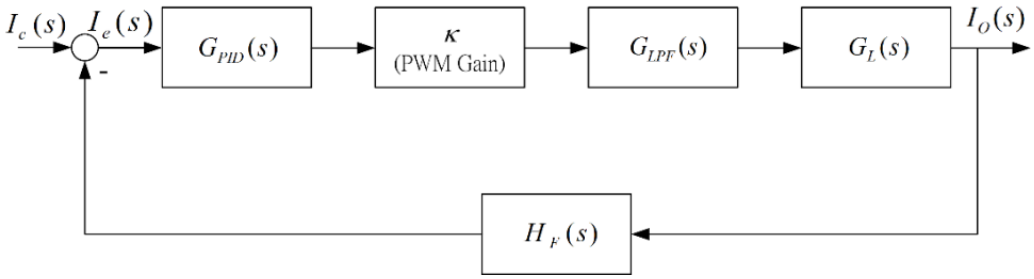

FIGURE 3. Block diagram of the closed loop system

Then the closed loop transfer function $T_{closed}(s)$ of the overall control system can be derived as

$$T_{closed}(s) = \frac{I_c(s)}{I_o(s)} = \frac{G_{PID}(s) \cdot k \cdot G_{LPF}(s) \cdot G_L(s)}{1 + G_{PID}(s) \cdot k \cdot G_{LPF}(s) \cdot G_L(s)} \tag{9}$$

where the $H_F(s)$ represents the feedback gain and is assumed as 1.

The controller is designed using the Ziegler-Nichols method with the assistance of Simulink/Matlab toolbox. Figure 4 shows the mathematical simulation model with Simulink. This is a mixed mode model simulation, where the transfer functions of each block are obtained as above in s-domain except the PID block, which is expressed in discrete z-domain. An AD converter (analog-to-digital converter) model, which is equivalent to a Zero-Order-Hold, is used to convert the analog feedback current to discrete data format with 50 KHz sampling frequency.

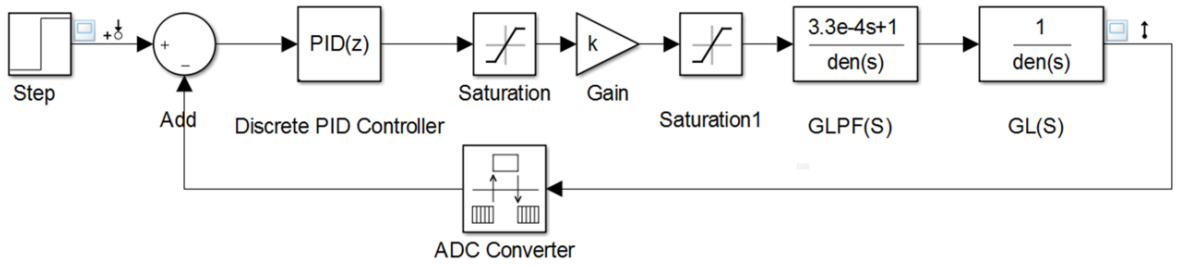

FIGURE 4. Simulink simulation model

The design goal to be achieved is listed in Table 2.

TABLE 2. Design specifications for time domain controller

Design Specifications of Time Domain Controller for the Fast Corrector Converter	
Maximum step size	0.1 A (1% of full scale 10 A output)
Rise time	< 100 μs
Overshoot	5% of the maximum step size
Settling time	< 100 μs within 3% of maximum step size

The K_P (proportional), K_I integral and K_D derivative values of the discrete PID controller are tuned according to the specification using the automatic tuning tool in Simulink. The z-domain transfer function of the PID controller using Forward Euler representation can be expressed as

$$G_{PID}(z) = P + I * \frac{T_s}{2}\frac{1}{z-1} + D * \frac{T_s}{2}\frac{z-1}{z} \tag{10}$$

$$K_P = P \quad K_I = I * \frac{T_s}{2} \quad K_D = D * \frac{T_s}{2} \tag{11}$$

where T_s is 20 μs, which is the 50 KHz sampling period. And the final tuned gain values are listed in Table 3.

TABLE 3. Tuned controller gain of the PID controller

Digital PID Controller Parameter		
K_P	K_I	K_D
111	0.4727	0.000125

The 0.1 A step response of the fast corrector magnet with the tuned PID controller values is shown in Figure 5. The rise time is at 63.26 μs, which is less than the 100 μs constraint and other specifications are also met with the tuned values.

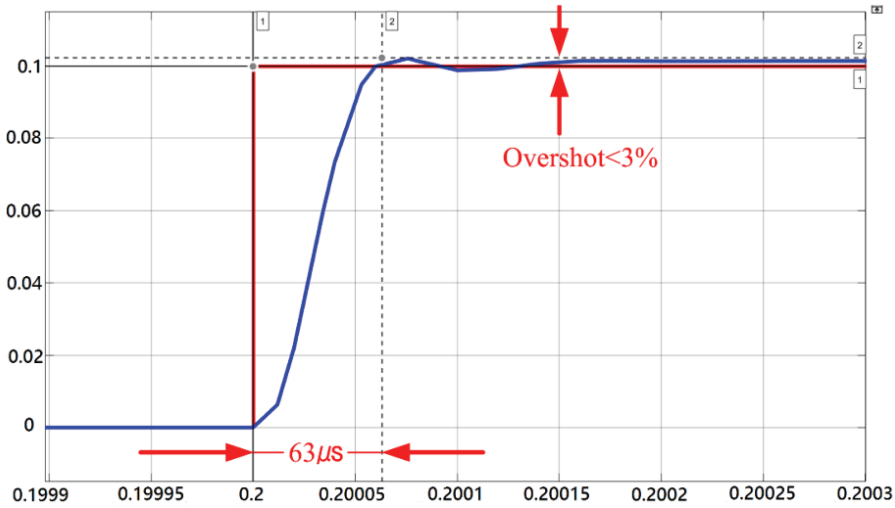

FIGURE 5. Simulated step response

In the following section, the hardware implementation of the digital TPS fast corrector will be explained in detail using the PID controller designed as derived above.

4. **Hardware Implementation.** The hardware architecture to realize the digital fast corrector power supply for the TPS ring is depicted in Figure 6. The digital power converter architecture consists of four building blocks: an NI embedded device with FPGA with digital IO ports, a single channel 18 bits zero-latency *successive approximation* (SAR) ADC, a four channel DAC converter, and fast corrector power converter stage connected to a fast corrector magnet load.

The embedded controller block is implemented with NI sbRIO-9606 single board computer equipped with Xilinx Spartan-6 LX45 FPGA and DIO (Digital Input Output) ports, which performs the major tasks: 1) Input/Output data communication to accept synchronous trigger, current command profile and PID control parameters through Ethernet protocol, 2) Digital PID block and PWM signals generation, 3) ADC read-back control and 4) DACs output control for system parameters monitoring.

All the PID parameters and current command are sent to hardware module from PC through the Ethernet. Figure 7 shows the virtual software interface for the overall proposed digital control scheme. The reference waveform generation, PI controller gains, waveform compensation parameters etc. are all accessible through the interface, which is realized by NI LabVIEW. The output current is measured and converted to voltage signal using 0.1 Ohm high precision shut resistor with 0.1% tolerance and ± 1 ppm/K temperature drift. The voltage signal is buffered and amplified with a gain of 10 and then amplified signal is sampled by zero-latency 18 bits ADS8382 ADC with 50 KHz

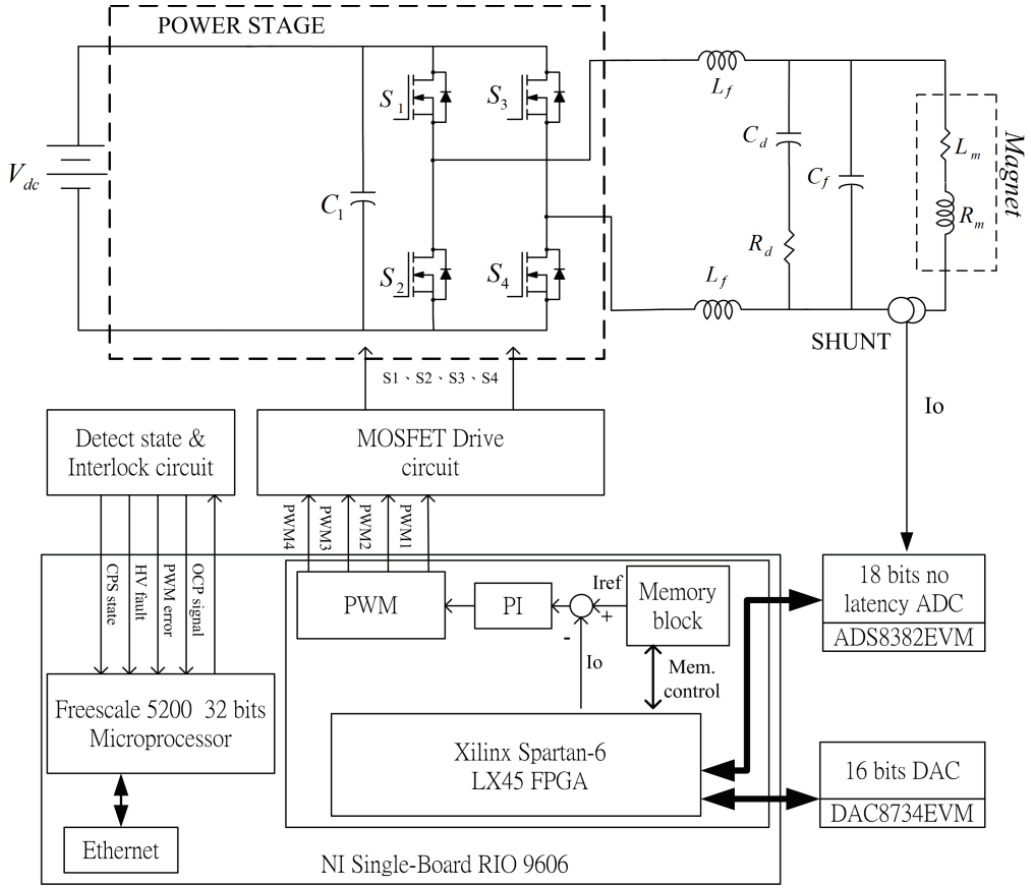

FIGURE 6. Hardware architecture of digital fast corrector power supply

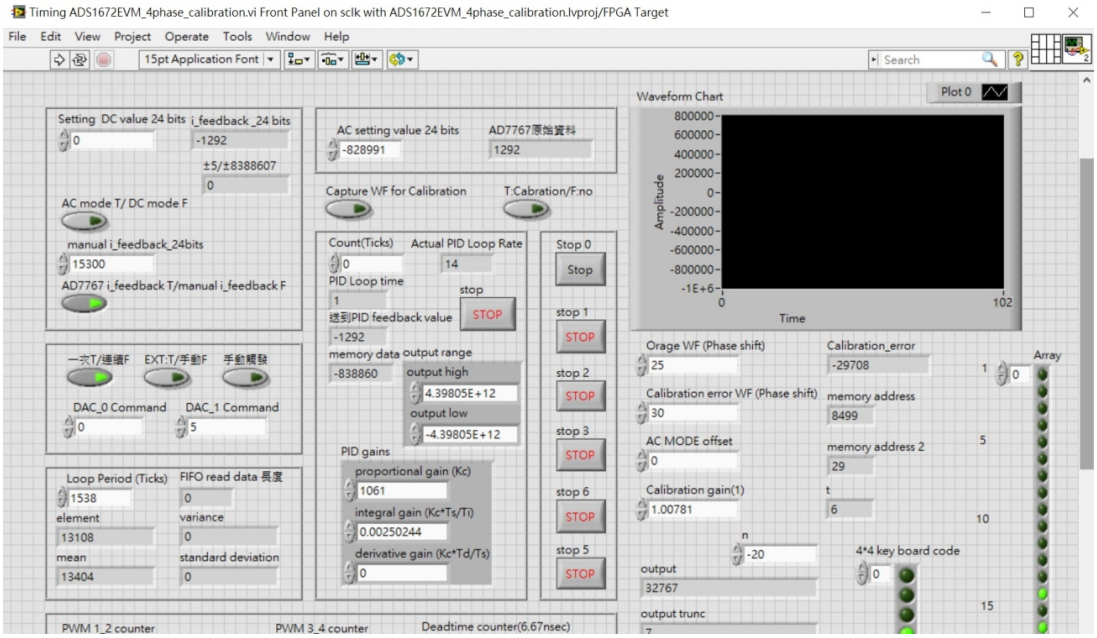

FIGURE 7. Virtual software control interface

sampling rate. The sampled current feedback data is retrieved back to the FPGA module to produce together with the current command the error signal to the digital PID block. The compensated command is calculated in PID and output to the PWM converter to generate the MOSFET switching signals for the H-bridge power stage. The four-channel

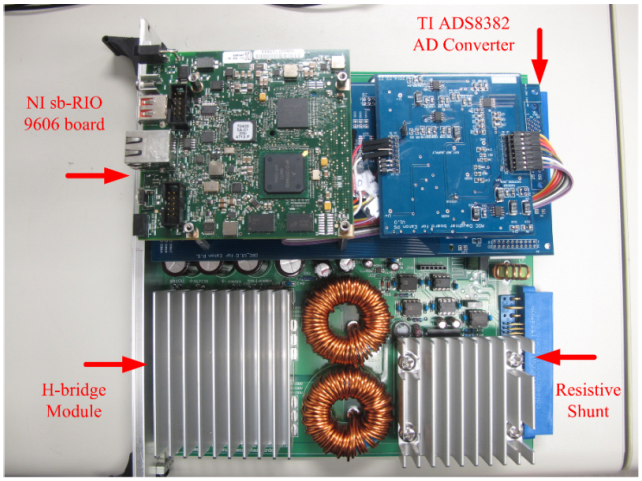

FIGURE 8. Photo of the realized prototype

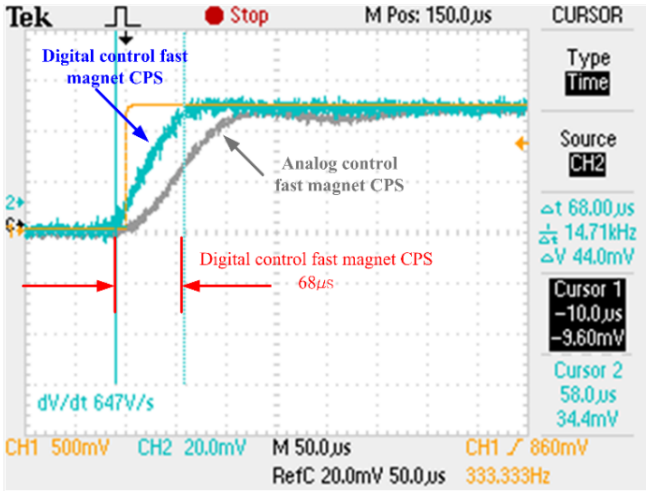

FIGURE 9. Measured step response

DACs are used to observe the command input and tracking error for easy comparison purpose through external digital oscilloscope. The photo of the realized digital fast corrector power supply is shown in Figure 8.

5. **Experimental Results.** To validate the designed power supply, a prototype has been built and tested if the performances meet the design requirements. For external output current measurement, high precision, wide bandwidth DCCT unit (ITZ 600 ULTRASTAB, Danfysik) is employed. The output current together with the current command output from DAC are monitored by oscilloscope to observe the designed performance. Figure 9 shows the 0.1 A step response. The yellow line is the 0.1 A step command from DAC while the grey and blue one are the current output of the prototype digital and existing analog version of fast corrector power supply respectively. The rise time of the proposed digital prototype is about 68 μs, which is slower than the 63 μs simulated result but still falls well within the specified 100 μs FOFB update interval. Furthermore, compared to 126 μs rise time of the analog version, the rise time of the digital prototype is significantly improved.

Also the frequency response of the experimental prototype is measured and compared to the simulation as shown in Figure 10. The -3 dB bandwidth of the prototype system is at 9.25 KHz. The measured phase margin is 160° and the gain margin is 10 dB, while the simulation results give 150° and 4.98 dB. From both the step and frequency responses,

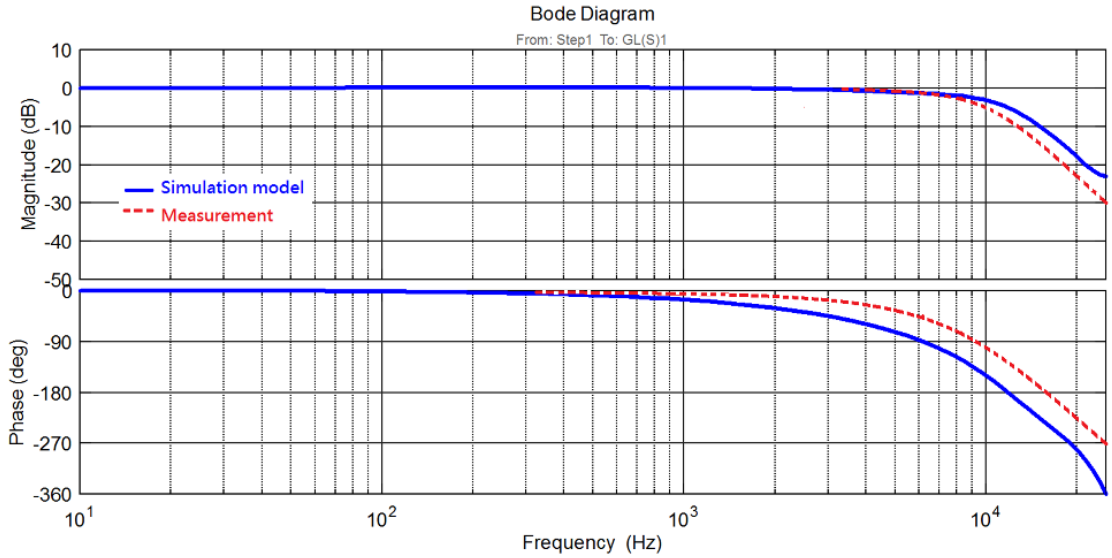

FIGURE 10. Frequency response of the simulated model and measured prototype

the performance of the proposed digital system is close to that of the mathematical model simulation and above all, meet the specifications as desired by the TPS FOFB system.

6. **Conclusion.** This paper presents a preliminary digital power supply design for the TPS storage ring fast corrector based on off-the-shelf embedded micro-controller board with FPGA and precision zero latency ADC. The proposed power supply control architecture is proved to be a compact current-mode controller with high bandwidth and fast transient. The experimental results also validate that the design satisfies the time-domain step response performance necessary for the FOFB system with 10 KHz update rate. With the capability of adjusting the discrete PID gains more efficiently to adapt to various types of magnet loads, this implies that a more robust and reliable performance can be expected than the analog design one. In the future, temperature compensation, improvement on the signal/noise ratio, and the protection circuit will be integrated into the digital control card to increase system reliability and friendly controllability.

REFERENCES

[1] C. C. Kuo et al., Commissioning of the Taiwan photon source, *Proc. of IPAC 2015*, Richmond, VA, USA, pp.1314-1318, 2015.
[2] O. Singh, Y. Tang and S. Krinsky, Orbit feedback at the NSLS, *Nucl. Instrum. Meth. A.*, vol.556, pp.267-279, 1998.
[3] P. C. Chiu, K. H. Hu, C. H. Huang, C. Y. Liao and K. T. Hsu, Preliminary beam test for TPS fast orbit feedback system, *Proc. of IPAC 2016*, Busan, Korea, pp.2930-2932, 2016.
[4] R. Garcia-Gil, J. M. Espi, F. Voelker, E. J. Dede and J. Castello, A novel four-quadrant power supply for low-energy correction magnets, *Nucl. Instrum. Meth. A.*, vol.510, pp.357-361, 2003.
[5] J. Zhao et al., Implementation of an FPGA controller for correction power supplies in heavy ion synchrotron, *Nucl. Instrum. Meth. A.*, vol.777, pp.167-171, 2015.
[6] K. B. Liu, Y. D. Li, B. S. Wang, K. T. Hsu and J. C. Hsu, TPS corrector magnet power converter, *Proc. of IPAC 2010*, Kyoto, Japan, pp.3269-3271, 2010.
[7] Y. C. Chien et al., Design of digital fast corrector power supply for TPS storage ring, *Proc. of ICEPE Conference*, 2016.
[8] M. Mohan, T. Undeland and W. Robbins, *Power Electronics*, 3rd Edition, John Wiley & Sons, Inc., 2003.