BIT-LINE LEAKAGE COMPENSATION AND CALIBRATION IN 65-NM SRAM DESIGN

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Abstract. *The bit-line leakage current becomes a challenge during the read operation as process technology scales. The increasing bit-line leakage current causes slow or even failed read operation of Static Random Access Memory (SRAM). This phenomenon becomes more serious when SRAM works in low power-supply voltage. This paper describes a new leakage current compensation and calibration technique. Even with large leakage current, correct data can be read out. In addition, it accelerates the read operation. Simulation results show that the speed of amplifying is increased by 60% compared with X-calibration (X-C) scheme. The sense amplifier response time of the proposed technique is shorter than that of the X-calibration technique under different process corners.*
Keywords: Bit-line leakage current, Compensation, Calibration, Sense amplifier, Response time

1. **Introduction.** As Complementary Metal Oxide Semiconductor (CMOS) process technology scales down, many critical design issues have already emerged. For example, larger process variation makes it difficult to match the symmetric devices, and increasing leakage current of transistor has negative effect on performance and data stability in today memory circuits [1-4]. It is necessary to design robust circuits in order to deal with these effects [5].

The threshold voltage of CMOS transistor is decreasing as the process scales down [6]; thus it brings larger leakage current [7]. This will lead to a lower speed of read operation. When the bit-line leakage current reaches a critical value, the read operation would even fail [8]. Bit-line leakage current becomes an urgent issue to tackle in high performance memory circuits [9].

1.1. **Basic principle.** Figure 1 is the conventional SRAM column. At the beginning of the SRAM to read operation, the bit-line pair (BL and $\overline{\text{BL}}$) is pre-charged to supply voltage (VDD). After pre-charged BL and $\overline{\text{BL}}$, write line (WL) is pulled high to turn on M1 and M2 transistors which are in the bit-cell. Meanwhile, the bit-line ($\overline{\text{BL}}$) will discharge which is connected to the store logic "0" as shown in Figure 2(a) [10]. Therefore, the bit-line pair would generate a voltage difference ΔV (we set $\Delta V = 150\text{mV}$) without the bit-line leakage current in relative short time [11]. After then, the sense amplifier predetermines the output result by sensing the differential voltage on two bit-line [12]. However, in Figure 2(b), the delay time increases due to the fact that the bit-line (BL) leakage current causes voltage drop. This will deteriorate the performance and decrease the operating frequency of the SRAM.
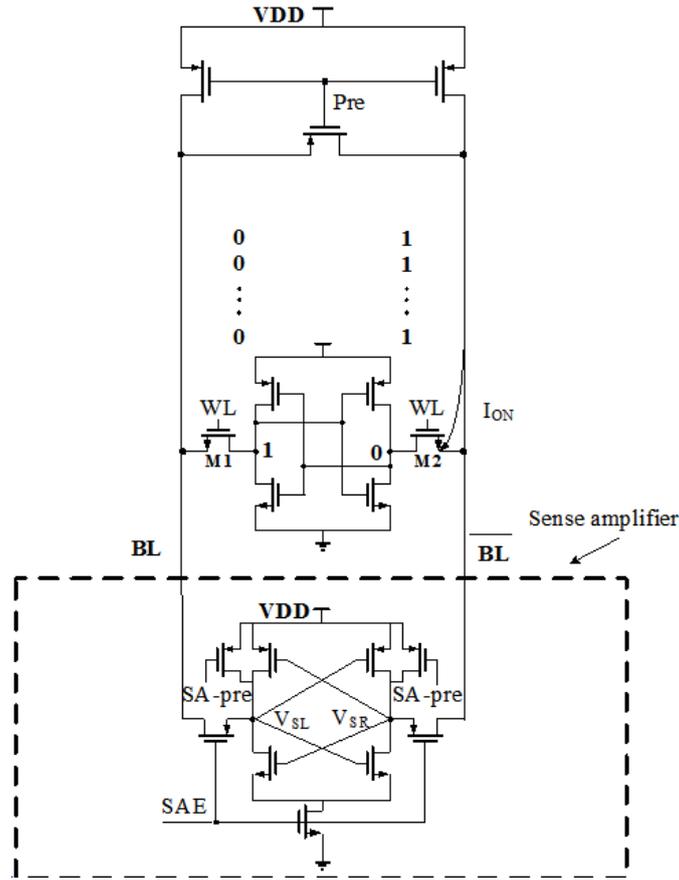
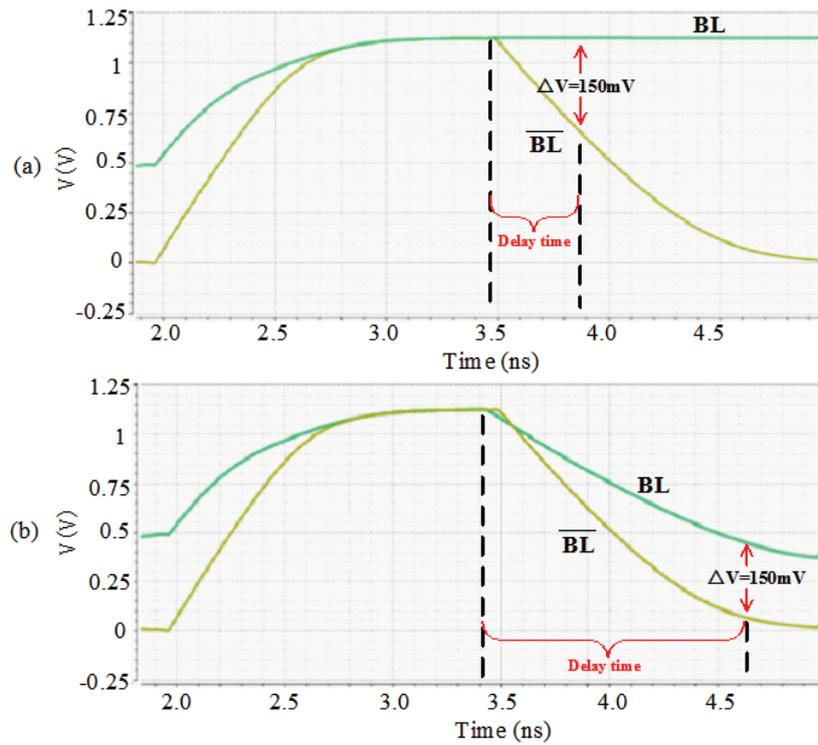FIGURE 1. Conventional SRAM column with bit-line leakage current

FIGURE 2. Waveforms of the bit-line pair for a conventional SRAM: (a) without leakage current, (b) with the bit-line leakage

1.2. **Current methods.** Several techniques have been proposed in [7,13,15]. A bit-line leakage current compensation scheme was proposed in [7], which detects the bit-line leakage current in pre-charge phases by a current-sensing circuit. The bit-line leakage current can be converted to a voltage stored in a capacitance. Then, similar amount of current compensates into the bit-line through a current mirror during read phases. However, the process variation has great influences on the current-sensing circuit, and this scheme is extremely susceptive to the variation of the threshold voltage. This scheme uses the transistor to detect the bit-line leakage current and inject the compensation, so the ability to withstand leakage current is limited. A bit-line leakage current equalization scheme proposed in [13] uses 8-transistors to inject equal current into the bit-line pair. Consequently, this technique eliminates the differential offset voltage due to leakage current. Nevertheless, the input voltage of sense amplifier drops to a low level which leads to deterioration of the sense amplifiers [14]. Besides, the scheme has about 40% area overhead. In addition, this scheme makes the bit-line voltage become lower than usual. A technique called X-C was proposed in [15]. This circuit uses capacitance to equilibrium offset voltage in the bit-line pair, and creates a reliable differential voltage in the input of the sense amplifier. Nevertheless, the performance of the scheme declines if the power-supply voltage is low because the equilibrium method makes the bit-line voltage become lower than usual [16]. This scheme uses subtracting to combat leakage current. When the bit-line drop is significant, the performance of SRAM will be affected.

This paper proposes a new compensation and calibration scheme to solve the bit-line leakage current problem for low voltage SRAMs. The main contributions of this work are as follows. 1) It is devoted to improving the speed of amplifying by raising the input voltage of the sense amplifier. When the bit-line leakage current is 43.3μA, the response time of compensation and calibration scheme is decreased by 49%, 32%, and 18% in tt, ff and ss process corners. 2) The proposed technique decreases the fluctuation of the response time of the sense amplifier when the leakage current varies.

The rest of this paper is organized as follows. In Section 2, the compensation and calibration scheme is described in detail. Simulation results and analysis are presented in Section 3. Finally the conclusions are given in Section 4.

2. **Bit-line Leakage Compensation and Calibration.** For deep submicron CMOS transistors, there is a sub-threshold current when the Metal Oxide Semiconductor (MOS) transistors are at the off state as shown in Figure 3. When the source-drain voltage (V_{DS}) is greater than 200mV, the sub-threshold leakage model is based on Equation (1) [17]:

$$I_{ST} = I_0 \exp \frac{V_{GS}}{\xi V_T} \quad I_0 = \mu_0 C_{ox} \frac{W}{L} V_T^2 \tag{1}$$

where I_{ST} is leakage current of CMOS, ξ is a non-ideal factor ($\xi > 1$), V_{GS} is the gate-source voltage, μ_0 is the zero-bias mobility, C_{ox} is the gate capacitance per unit area, W/L is the gate aspect ratio, and V_T is the thermal voltage ($V_T = \frac{kT}{q}$).

Suppose there are N bit-cells attached to the bit-line of the SRAM, and only one bit-cell stores logic "1" and all others ($N - 1$) store logic "0" and then the bit-line leakage current ($I_{Leakage}$) is:

$$I_{Leakage} = (N - 1) \times I_{ST} = (N - 1) \times I_0 \exp \frac{V_{GS}}{\xi V_T}$$
$$= (N - 1)\mu_0 C_{ox} \frac{W}{L} V_T^2 \exp \frac{V_{GS}}{\xi V_T} \tag{2}$$

When the MOS transistor is at the on state, the source-drain current (I_{DS}) is:

$$I_{DS} = I_{ON} = \mu_0 C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \right) \tag{3}$$

where V_{TH} is threshold voltage, and I_{ON} is read current.

The amount of the bit-line leakage current depends on how many bit cells are in one SRAM array column. Therefore, there are two cases: 1) the bit-line leakage current ($I_{Leakage}$) is less than the read current (I_{ON}); 2) $I_{Leakage}$ is greater than the read current I_{ON}. In the first case, the time for generating the differential voltage increases which is proportional to the bit-line leakage current. In case 2, the read operation fails because the data is wrong. Therefore, the purpose of this paper is to eliminate the impact of leakage current on bit line voltage.
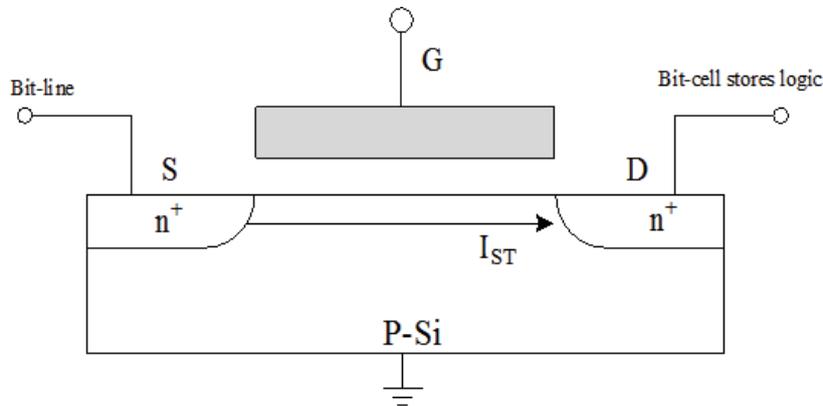

FIGURE 3. Leakage current of MOS transistor in off state

2.1. **Circuit structure.** The proposed circuit uses two coupling capacitors in the bit-line pair, several transistors, and two additional control signals, CON1 and CON2 which control the operation of the compensation scheme, as shown in Figure 4.

The compensation and calibration scheme compensates the offset voltage of the bit-line pairs before read phase. The ΔV_{SA} is no longer equal to the voltage difference between BL and $\overline{BL}$, which does not vary as the bit-line leakage current changes. In this way, the input voltage of the sense amplifier is the same as that without bit-line leakage current, which improves the performance of the sense amplifier.

2.2. **Circuit operation and waveforms.** Figure 5(a) shows the transient waveforms of the bit-line pair and input pair of the sense amplifier (SA_in and $\overline{SA\_in}$) when the leakage current exists in one bit-line (BL). Figure 5(b) shows the waveforms of control signals.

The read operation of the SRAM with the compensation and calibration circuitry can be divided into the following three phases: pre-charge phase, detection phase, and compensated reading phase.

1) Pre-charge phase: the bit-line pair is charged to VDD by the pre-charge circuitry. At this moment, CON1 and CON2 are high (off state), and the block of compensation and calibration circuit does not work. Therefore, the bit-line voltage is:

$$V_{BL} = VDD \quad V_{\overline{BL}} = VDD \tag{4}$$

2) Detection phase: the pre-charge circuit is turned off, and CON1 and CON2 are low (Positive Channel Metal Oxide Semiconductor (PMOS) is conducted). Due to the bit-line leakage current, the voltage of bit-line drops down. The voltage transfers from the bit-line to one side of the capacitor, and another side of the capacitor connects to the VDD. Finally, the node which is connected to the sense amplifier will form a compensation voltage. Assume that the voltage drop due to the leakage current is named as leakage voltage ($V_{leakage}$), each node voltage is:
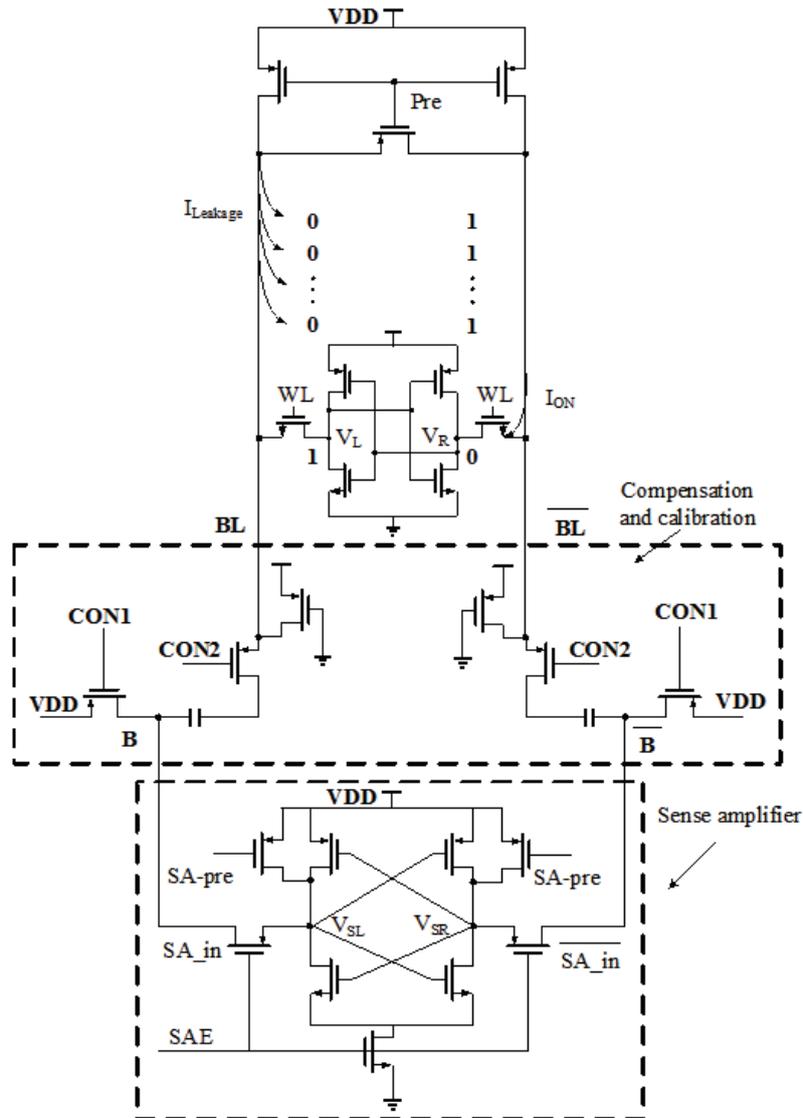
$$V_{BL} = VDD - V_{leakage} \quad V_B = VDD \tag{5}$$

FIGURE 4. Schematic of the compensation and calibration circuitry

3) Compensated reading phase: turn off the PMOS with CON1. And then, the compensation voltage is added to the bit-line voltage. Therefore, the offset voltage is cancelled in the input pair of the sense amplifier in this phase. Suppose that the voltage drop due to reading the data is named as read voltage (V_{read}), each node voltage is:

$$V_{BL} = VDD - V_{leakage} \quad V_{\overline{BL}} = VDD - V_{read}$$
$$V_{\overline{B}} = VDD - V_{read} \quad V_B = VDD - V_{leakage} + (V_{leakage}) = VDD \tag{6}$$

The input voltages of the sense amplifier are $V_{\overline{B}}(VDD-V_{read})$ and $V_B(VDD)$. Therefore, this circuit eliminates the effects of leakage current.

In order to clearly demonstrate the operation of the three phases, we use approximate values to describe the voltage change of each node which are shown in Table 1. The bit-line pair is charged to 1.2V in pre-charge phase. The third row of the table shows the detection phase. The bit-line voltage of BL drops down and ultimately dives to 1.0V due to bit-line leakage current, but another bit-line $\overline{BL}$ maintains the initial voltage 1.2V. At the same time, the nodes B and $\overline{B}$ are connected to 1.2V. Thus, the node B voltage is 0.2V higher than another side of the capacitor in bit-line BL. Finally, the voltage of the bit-line $\overline{BL}$ drops down from 1.2V to 1.05V because of the read current in compensated reading phase, and the BL maintains 1.0V. Through the capacitor, the voltage of B becomes 1.2V
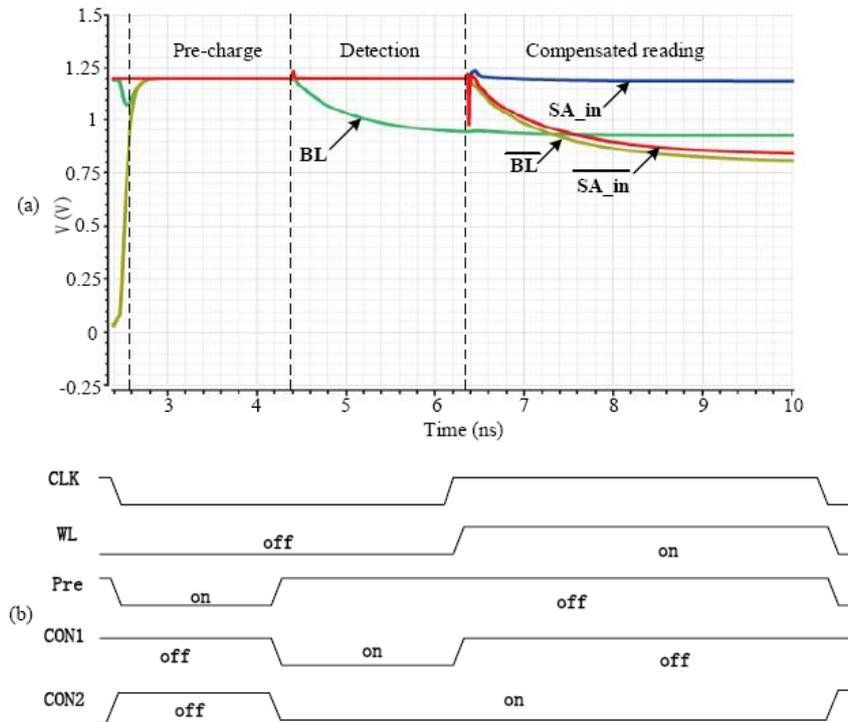
FIGURE 5. (a) Waveforms of the bit-line pair and input pair of the sense amplifier, (b) read timing diagram of the compensation calibration circuitry

TABLE 1. Change of node voltage at each stage

	BL	$\overline{\text{BL}}$	B	$\overline{\text{B}}$	SA_in	$\overline{\text{SA\_in}}$
Pre-charge (V)	1.2	1.2	–	–	–	–
Detection (V)	1.2→1.0	1.2	1.2	1.2	–	–
Compensation and Read (V)	1.0	1.2→1.05	1.0→1.2	1.2→1.05	1.2	1.05

and the voltage of $\overline{\text{B}}$ becomes 1.05V. The offset voltage is eliminated from the input pair of the sense amplifier.

3. **Simulation Results.** The aforementioned technique has been implemented in a 128 × 64 SRAM with 65-nm SMIC CMOS process technology. The output data is obtained by sense amplifier. So, the sense amplifier response time is important in read operation. The definition of the response time is from the moment that the enabling signal of sense amplifier activates to the time when the data is read out.

The sense amplifier response time relates to the input voltage difference and voltage level. If the voltage difference is smaller and lower, the response time is longer. Bit-line leakage current can cause more drop in the sense amplifier input voltage. The relationships of the response time and the amount of bit-line leakage current are shown in Figure 6. The response time is increased slowly when the leakage current is less than 20μA. While the bit-line leakage current is increased from 40μA to 50μA, the response time of X-C scheme was nearly doubled but that of the compensation and calibration scheme changed slightly. The simulation results show that the compensation and calibration scheme can improve 60% in terms of the response time compared with the X-C scheme under the maximum tolerant bit-line leakage.

Figure 7 shows the comparison results under several process corners between X-C scheme and compensation and calibration scheme. In ff process corner, the response
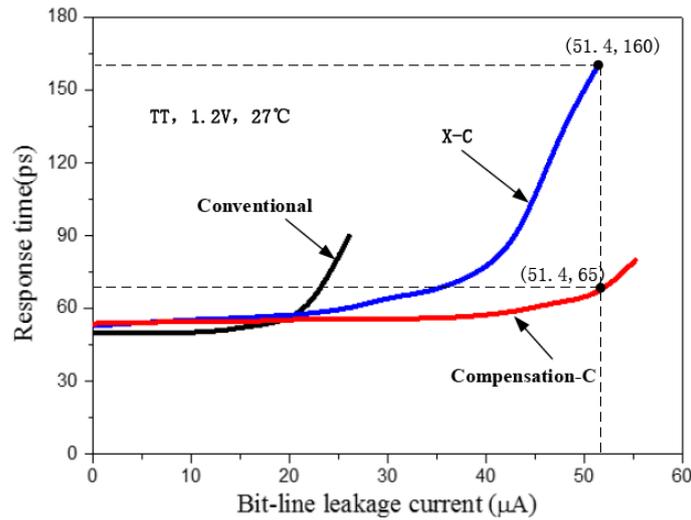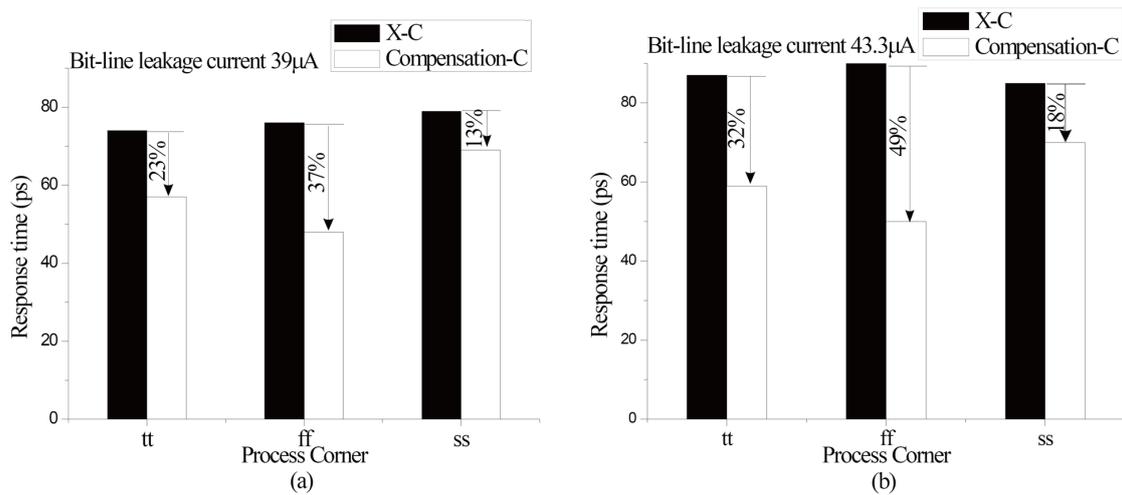
FIGURE 6. Bit-line leakage dependence of the SA response time

FIGURE 7. Response time in different process corners if (a) the bit-line leakage current is 39μA, (b) the bit-line leakage current is 43.3μA

time of compensation and calibration scheme decreases by 37% when the bit-line leakage current is 39μA as shown in Figure 7(a). If the leakage current increases to 43.3μA, this ratio increases to 49% in Figure 7(b).

Figure 8 shows the Monte Carlo simulation distributions of response times. With the same bit-line leakage current, the response times of compensation and calibration scheme are swung from 53ps to 56ps, as shown in Figure 8(a), but the X-calibration scheme is around 63ps, as shown in Figure 8(b). This again shows that the response time of compensation and calibration scheme is shorter than the X-calibration scheme.

4. **Conclusions.** In this paper, a new method has been proposed to solve the problem of bit-line leakage current. This method does not reduce the input voltage level of sense amplifier. Since lower input voltage affects the response time of SA and the read operation time, this proposed circuit can improve about 60% performance of sense amplifiers with large leakage current. When the bit-line leakage current is 39μA, the response time of compensation and calibretion scheme is decreased by 37%, 23%, and 13% in different process corners. As the leakage current increases to 43.3μA, the response time is decreased to 49%, 32%, and 18%, respectively. In addition, Monte Carlo simulation results prove the reliability of compensation and calibration scheme in 65-nm process. The response
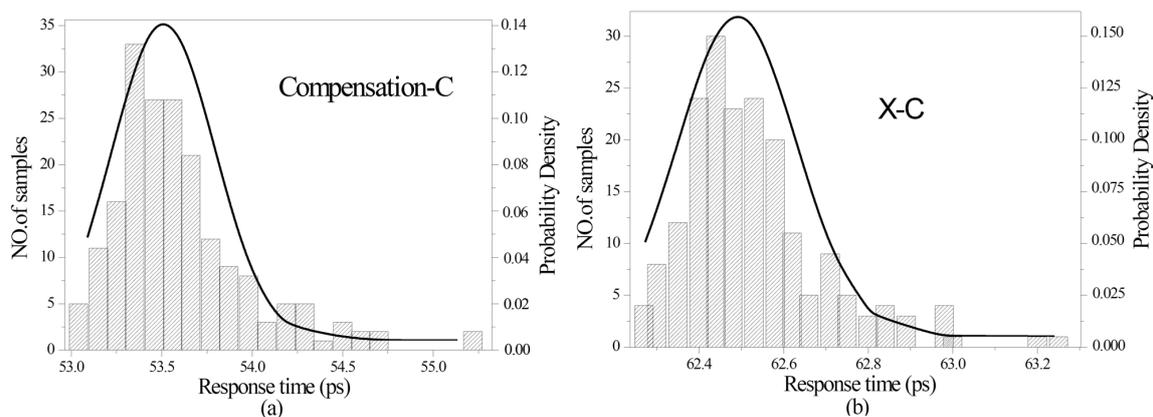
FIGURE 8. Monte Carlo simulation of the response time, (a) compensation and calibration scheme, (b) X-calibration scheme

time of compensation and calibration scheme is around 53ps, but that of the X-calibration scheme is around 62ps.

However, as the leakage current increases, the response time of compensation and calibration scheme becomes large. Therefore, the research topic in the future is to improve the structure to tolerate more leakage with less area overhead.

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