ICIC Express Letters
Part B: Applications
Volume **8**, Number **5**, May **2017**

ICIC International ©2017 ISSN 2185-2766
pp. **827–834**

DIGITAL LEARNING CONTROLLER DESIGN FOR THE BOOSTER RING AC POWER SUPPLIES IN TAIWAN PHOTON SOURCE

Yuanchen Chien, Chenyao Liu, Yongseng Wong, Kuobin Liu and Baosheng Wang

Department of Power Supply Group
National Synchrotron Radiation Research Center
No. 101, Hsin Ann Road, Hsinchu 300, Taiwan
wang.bs@nsrrc.org.tw

Received December 2016; accepted March 2017

Abstract. *The AC power supplies of the booster ring must function with high precision and accuracy in both DC and AC modes in the recently commissioned Taiwan Photon Source (TPS). The performance requirement is much stricken particularly in the AC mode. While in the booster beam energy ramping, the current ramping waveforms of the AC power supplies should keep in track closely with the desired current profiles, where precise phase and amplitude related are a must in order to maintain good electron beam energy boosting efficiency. Currently, all booster AC power supplies are built with analogue PI controllers. Current ramping waveforms data are prepared and converted to analogue signals and then sent to all booster power supplies synchronously. Here we propose a hybrid iterative learning control (ILC) algorithm combined with discrete PID feedback controller with the objective to minimize the tracking error with iterative learning automatically and the signal integrity problem inherent in analogue controller, so that boosting the beam energy might become more reliable. The proposed digital controller platform has been implemented and applied to the TPS corrector magnet power supply and slow corrector magnet load with success.*

Keywords: Booster, AC current tracking, Iterative learning control, PID control, Power supply

1. **Introduction.** The booster ring was successfully commissioned and the electron beam was accelerated from 150 MeV to 3 GeV with repetition rate 3 Hz on December 16, 2014. At the end of 2015, the stored-beam current of TPS had attained 521 mA, beyond design goal 500 mA [1,2].

Figure 1 shows the 3 Hz ramping waveforms of the booster AC power supplies. There are total five AC power supplies in the TPS booster ring which must be operated in 3 Hz ramping. They are one dipole magnet power supply and four kinds of Quadruple magnets power supplies, Q1, Q2, QM and QF respectively. As shown in Figure 1, at the injection point, the 150 MeV electron beam is injected from the linear accelerator (LINAC) to the booster ring. And along with the picking-up of beam energy each time the beam travels through the booster RF cavity, the magnet flux of the dipole and quadruple magnets should also be increased accordingly to match the beam energy in order to keep the beam travel in the defined orbit. Since the allowable beam orbit in the booster ring is small in size both in the vertical and horizontal axis inside the beam duct, the importantance of stable AC power supplies cannot be overstated. Each power supply has to perform with precision and good reproductivity especially at the injection point.

Currently, the controlling and monitoring of the booster AC power supplies are executed in the Experimental Physics and Industrial Control System (EPICS) control unit [3]. The overall system works synchronously with the timing clock derived from the RF operating frequency to make sure the phase lags among the AC power supplies are guaranteed.

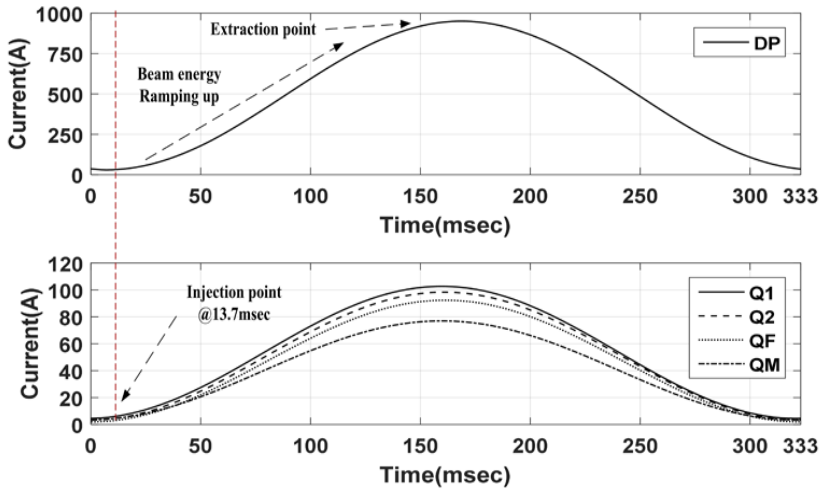

FIGURE 1. TPS booster power supplies current ramping profiles

The waveform data are converted to analogue differential signals with DAC (20 bit) and distributed to all booster ramping power supplies.

The current booster dipole and quadruple AC power supplies are contracted to and built by Eaton [4]. In quadruple power supplies, full-bridge is used to construct the converter stage. In the switching topology, only a single DC voltage bank and four IGBTs switching modules to form the full bridge are implemented. The dipole power supply employs full-bridge topology too. Because it has much larger output current rating than that of the quadruple ones, the full bridge topology is formed by two DC voltage bank and connecting two identical 2-Quadrants IGBT modules in parallel. The switching frequency of dipole and quadruple converters is designed at 2 kHz and 40 KHz respectively.

The energy boosting efficiency of the booster ring relies on the independent tracking error between the input command and measured output current waveform of the dipole and quadruple power supplies. The tracking performance of the booster AC power supplies are measured by normalized individual tracking error (NRE). The NRE is the difference of the current out waveform of each AC converter at every time sample following the first 3 Hz cycle compared to that of the subsequent ramping cycles. The individual indicator is to check if the DPS and QPS's current stability is consistent each time the ramping waveform is repeated. The NRE is defined as follows:

$$NRE(i)(t) = \frac{I_{dipole}(i)(t) - I_{dipole}(1)(t)}{I_{dipole}(1)(t)} \times 100\% \tag{1}$$

where i represents the cycle iteration number and t is the sampled instance.

Because of the various booster dipole and quadruple magnet loading, different building architectures of the booster dipole/quadruple power supplies and the analogue control scheme which is vulnerable to electrical noise, keeping the tracking error well below the desired NRE 0.2% at the injection point is a difficult challenge in the long run. For the analogue PI controller gain values are susceptible to the temperature drift, component tolerance, component aging and EMI noise problems. Besides, waveform compensation strategy called proportional and time shift compensation are currently adopted to reduce the NRE, which is similar to ILC algorithm except that the phase lag between the current command and actual current feedback has to be estimated first manually but not automatically compensated [5]. Estimated phase lag may vary with temperature and is error-prone if done manually.

In this paper, a hybrid P-type iterative learning control (ILC) and discrete PID controller platform is developed in hope to reduce the NRE further automatically by avoiding the disadvantages which the current analogue controller and manual estimation of phase

lag might incur. In order to test the functionality of the proposed digital controller platform, power converter stage and magnet load of slow corrector magnet are used to verify its performance because the corrector power converter employs the same converter topology like those of the AC dipole/quadruple ones. The slow corrector power converter is capable of delivering ±10 A at ±50 V [6]. First, the digital controller hardware platform is described. Second, a hybrid P-type ILC with discrete PID controller design is introduced. And last, the experimental results are presented.

2. **Digital Control Platform Hardware.** The digital controller platform has been implemented utilizing commercially available embedded microcontroller with FPGA (Field Programmable Gate Array) to reduce the development cost and time. The digital platform schematic is depicted in Figure 2. The digital controller platform consists of an embedded microprocessor board with FPGA and a DCC card (digital data converter card). The embedded microprocessor board (NI sbRIO-9606) has an FPGA (Xilinx Spartan 6) in it and is aimed to perform the functions such as data communication with central controller responsible for downloading current ramping waveforms. In the FPGA, P-type ILC control block, discrete PID controller and PWM algorithm are implemented. In addition, the block memories in the FPGA are utilized as the parameter memories for ILC. The P-type ILC control gain, PID controller values are downloaded through the embedded microcontroller from the external EPICS node from the centre booster control unit. The EPICS node is also responsible for sending trigger to synchronize all the AC power supplies' current output automatically. The DCC card is consisted of PWM switching signals isolation buffers, 16 bits multi-channels Digital-to-Analogue converter DAC, a 24 bits precision SAR Analogue-to-Digital converter (ADC) and current feedback DCCT (Direct-Current Current Transformer) modules. DCC executes the digitization of the current feedback signal coming from a DCCT. Ultra-high precision 24 bits ADC is used to serve the data conversion purpose. Also, switching signals generated by PWM block to control the IGBTs or MOSFETs of the full bridge are buffered and galvanically isolated before sending them to control the switches. The DACs are programmed to output system parameters like feedback current, current command and others for easy monitoring and debugging.

3. **Hybrid P-Type ILC and Discrete PID Controller Design.** In this design stage, phase lag and tracking error reduction method based on hybrid P-type ILC and PID feedback controller will be presented.

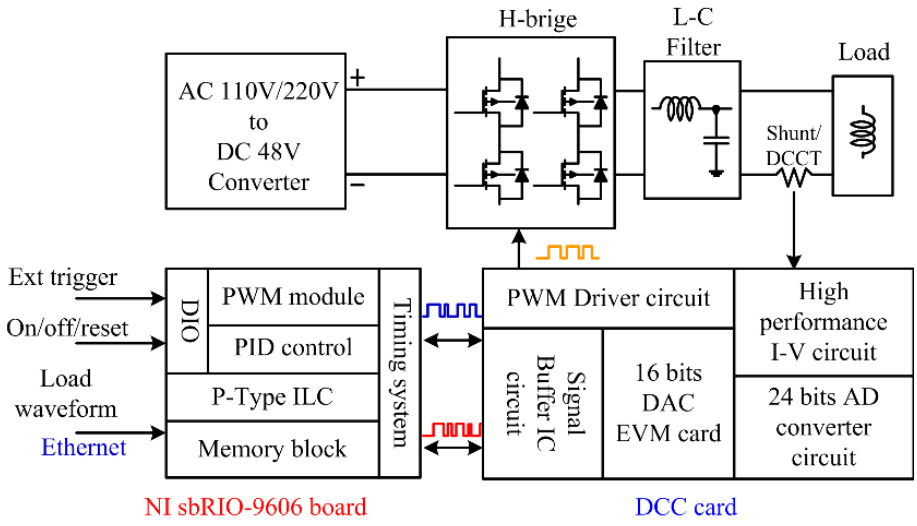

FIGURE 2. Digital controller platform functional blocks

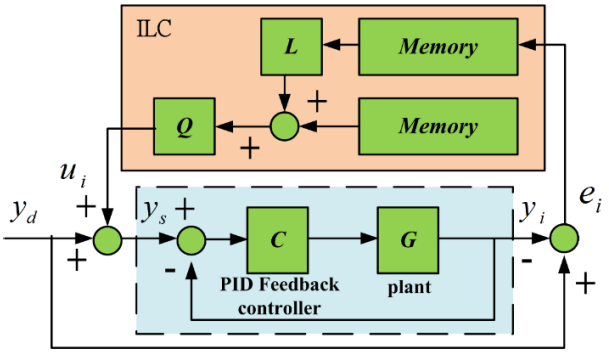

FIGURE 3. ILC feedforward with PID feedback control

Figure 3 shows the iterative learning method functional block diagram. This error reduction algorithm is called indirect iterative leaning control (ILC), which is commonly used to cooperate with existing feedback controller loop like PID to minimize tracking error in repeated processes [9,10]. In the previous literatures, this kind of learning control has been applied widely to industrial robots, chemical batch process and many others which perform repeated action. Applications to AC-DC/DC-DC power converter are still rare using this hybrid technique. Few articles are found to use ILC in UPS inverter to reduce the periodic disturbance [11,12]. Since the 3 Hz the current ramping of the TPS booster ramping behaves like a repeated process, the ILC ideal is proposed here to minimize the tracking error of the ramping current iteration by iteration. The proposed algorithm can be seen as a feedforward control to update the current set-point to minimize the tracking error between the reference current command and the actual current output waveform. As shown in Figure 3, in the ith iteration, the updated set-point $y_s(i,k)$ is given by

$$y_s(i,k) = y_d(k) + u(i,k) \tag{2}$$

where y_d is the desired current profile, u is the set-point modification term from ILC and k is the time sample within iteration i. The ILC update law is expressed as

$$u(i+1,k) = Q(u(i,k) + L(e(i,k+1))) \tag{3}$$

where Q and L are called the Q filter and learning gain respectively. In this paper, Q is not employed and L is set as a simple gain value to be changed for fast and stable convergence. Hence, the ILC algorithm is reduced to

$$u(i+1,k) = u(i,k) + L \times e(i,k+1) \tag{4}$$

This type of ILC update algorithm is called P-type ILC, which is the most commonly used method with solid robustness, if the gain L is properly chosen [13].

First, a discrete PID feedback controller which stabilizes the entire closed loop is developed. Second, proper L values are explored and evaluated for convergence. The circuit model of hybrid learning control is depicted in Figure 4.

The upper part is full-bridge converter stage. The lower left part implements P-type the ILC algorithm, where err_mem, u_mem and u_mem_old are the memory for setting error and set-point update term respectively for ILC. In the lower right discrete PID controller and PWM generator are located.

3.1. **PID controller design.** The simplified circuit diagram of the slow corrector power supplies is shown in Figure 5. V_{dc} is the DC voltage across the DC bus after the AC line input rectification. The energy is stored in DC bus capacitor bank C_1. The switchers convert the DC bank voltage to the desired current output using Pulse-Width-Modulation (PWM) method. The switching stage is mainly composed of MOSFETs switches forming the H-bridge in two legs ($S1/S2$ and $S3/S4$) and a damped outputripple low pass filter.

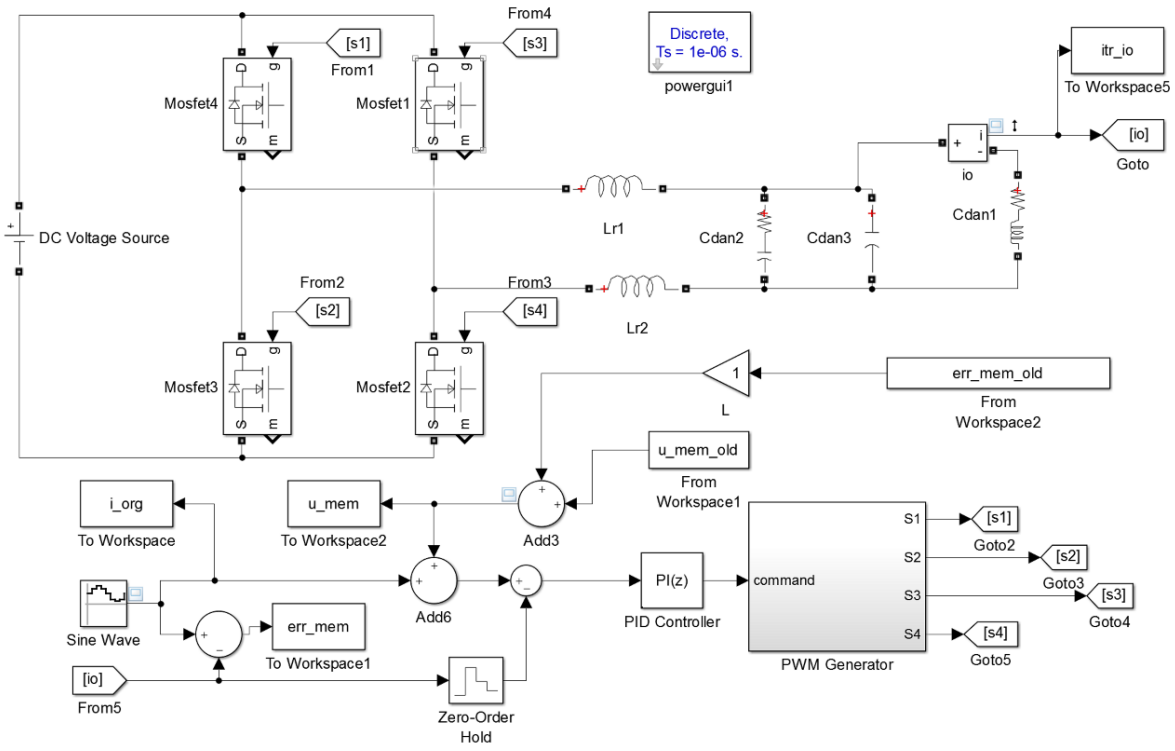

FIGURE 4. Hybrid P-type ILC and PID regulation circuit simulation model

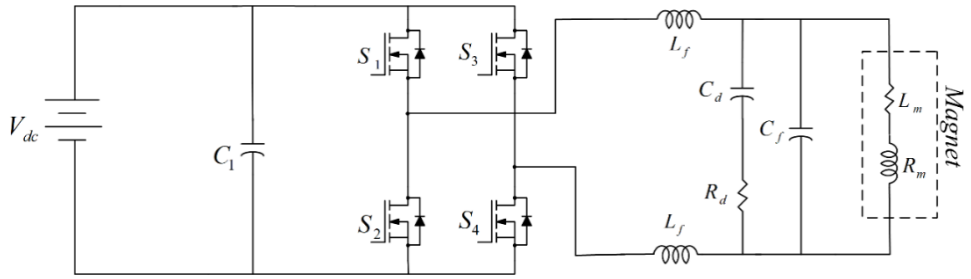

FIGURE 5. Power stage of TPS slow corrector

TABLE 1. TPS slow corrector power supply design parameters

TPS Slow Corrector Converter Specifications	
L_f	200 μH
C_f	2.5 μF
C_d	33 μF
R_d	10 Ohm
L_m	54.9 mF
R_m	0.601 Ohm

The adopted PWM switching method is complementary unipolar switching for it exhibits low switching loss and, above all, the output voltage frequency is twice that of the carrier frequency, which makes the design constraint on the output ripple low pass filter more relaxed. The circuit parameters of the slow corrector power converter are listed in Table 1. And the mathematical model diagram of the overall closed-loop control system is depicted in Figure 6.

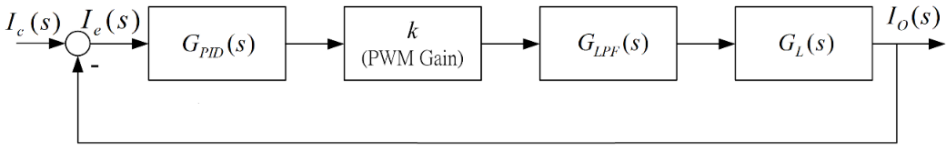

FIGURE 6. Mathematical model of the closed loop system

The s-domain transfer functions of closed loop control system are defined as follows:

$$G_{PID}(s) = K_P + K_I \frac{1}{s} + K_D s \tag{5}$$

$$G_{LPF} = \frac{1 + C_d R_d s}{1 + C_d R_d s + (L_f C_f + L_f C_d)\, s^2 + R_d C_f C_d L_f s^3} \tag{6}$$

$$G_L(s) = \frac{1}{R_m + L_m s} \tag{7}$$

$$k = \frac{V_{dc}}{V_{tri}} \tag{8}$$

where $G_{PID}(s)$, G_{LPF} and $G_L(s)$ are the transfer functions of the PID compensator, output low pass filter and slow corrector magnet respectively, while k is the PWM gain, which can be derived from a period of the PWM cycle [7].

Ziegler-Nichols method is adopted to design the PID controller with simulation software Simulink toolbox [8]. The mathematical simulation model built with Simulink toolbox is shown in Figure 7. A precision AD converter (analogue-to-digital converter) block followed by a discrete delay of latency d, is to simulate the data latency which the high precision 24 bits AD converter will introduce. The sampling frequency is set as 40 KHz, similar to that of quadrupole power supplies.

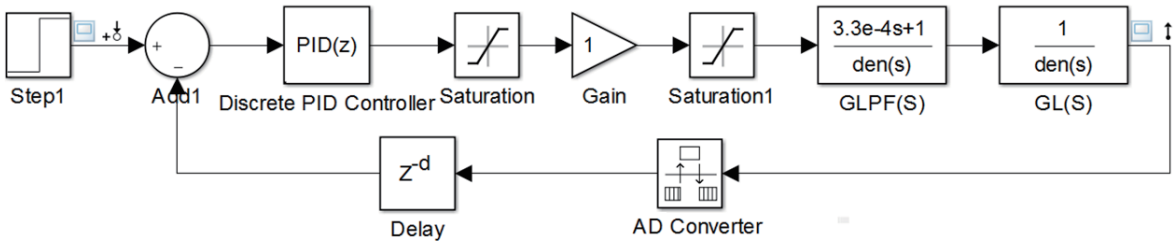

FIGURE 7. SIMULINK simulation model

For the AC power supplies work at only two modes, which are DC and AC 3 Hz mode, power converter's bandwidth is set at around 500 Hz, not too low to track the 3 Hz waveform command and not too high to minimize the unnecessary noise coming with high bandwidth. Moreover, to avoid any high frequency oscillation, step response overshoot is not allowed. Steady state is also required to be zero for precision waveform tracking.

The designed discrete transfer function of the PID controller by Trapezoidal method can be represented by

$$G_{PID}(z) = P + I * \frac{T_s}{2} \frac{z+1}{z-1} + D * \frac{1}{T_s} \frac{z-1}{z} \tag{9}$$

T_s is the period of the 40 KHz sampling frequency. The tuned controller gain P, I and D values are 29.29, 274.13 and 0.001 respectively. The -3 dB bandwidth is at 545 Hz, the phase margin is 30.7 dB and gain margin is 90 deg.

3.2. **ILC learning gain selection.** In this stage, with the discrete PID controller designed above, L values are tested with simulation to check if system will converge and how fast it does. Matlab script file is used to call the circuit model as shown in Figure 4 repeatedly for tracking error evaluation. The tracking error current at the 13.7 ms injection point with 20 iteration ramping cycles when learning gain L is set as 0.1, 0.5 and 1 respectively is depicted in Figure 8. It is shown that as L is set 1, it take only 3 iterations or 3 Hz cycles for the error current to converge to near zero.

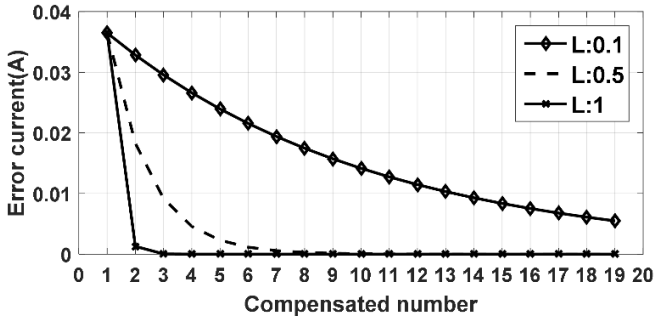

FIGURE 8. Tracking error current convergence curves with L set at 0.1, 0.5 and 1

4. **Experimental Results.** The current waveforms of the desired set-point and current feedback together with the NRE error when only PID regulator works but the ILC function is turned off are shown in Figure 9. The current command, which is a 3 Hz profile with 10 A peak amplitude, is applied to the proposed digital control platform with TPS slow corrector power stage and load. Due to the magnet load's inductance, significant phase lag is observed between these two waveforms, which make the NRE error obvious when current is small.

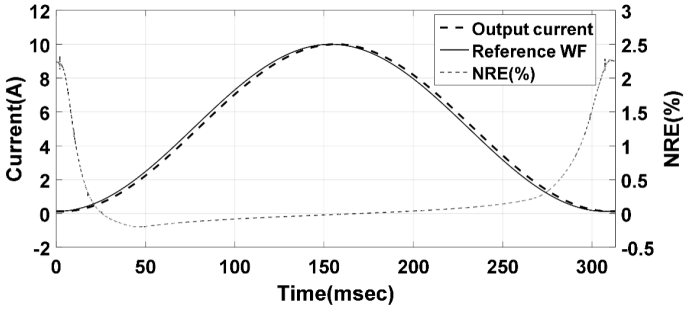

FIGURE 9. Reference and output waveforms and NRE with PID regulation only

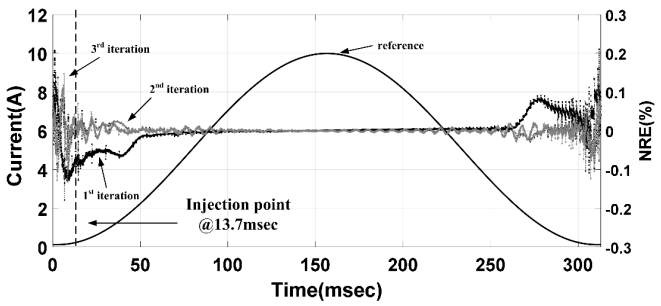

FIGURE 10. Reference and output waveforms and NRE with P-type ILC turned on

While the ILC function is enabled with the learning gain L set at 1, waveforms of the reference input and current feedback and the NRE error after 3 iterations are illustrated in Figure 10. The phase lag between the reference and current feedback is compensated automatically and the NRE is greatly decreased, requiring only 3 iterations for the NRE to fall below 0.1% at the 13.7 ms injection point during the 333 ms period of the 3 Hz ramping frequency for the TPS booster energy ramping.

5. **Conclusion.** In this paper, a digital regulation architecture combining a traditional PID feedback loop with P-type iterative control feedforward controller for the TPS booster ramping power supplies is presented. The preliminary prototype is first applied to a TPS slow corrector power converter to experiment if the proposed platform is able to meet the specified requirements. Both the simulation and experimental results show that this digital learning control platform is able to minimize the NRE cost function effectively. The current output waveform will converge to the desired current command in a few leaning iterations with the hybrid algorithm so that the NRE error is reduced from the desired 0.2% to less than 0.1% at the injection point during the 3 Hz ramping cycle. The proposed platform has shown great potential of improving the phase and tracking error of the booster AC power converters with similar topology operating in a repeated current command manner. In the future, the proposed digital regulation architecture will be applied to booster Quadruple magnet power supplies first and last the Dipole magnet power supply to verify if the proposed method is valid to serve the purpose to minimize the NRE error and hence improve the booster ring efficiency.

REFERENCES

[1] H. J. Tsai et al., Hardware improvements and beam commissioning of the booster ring in Taiwan photon source, *Proc. of the 6th International Particle Accelerator Conference*, Richmond, VA, USA, pp.1741-1743, 2015.

[2] Y. C. Chien et al., Status of AC power supplies for TPS booster ring, *Proc. of the 6th International Particle Accelerator Conference*, Richmond, VA, USA, pp.3203-3205, 2015.

[3] C. Y. Wu et al., Control interface and functionality of TPS booster power supply, *Proc. of the 6th International Particle Accelerator Conference*, Richmond, VA, USA, pp.1094-1096, 2015.

[4] Eaton, *TPS Booster Quadrupole Power Supply Installation, Operation and Maintenance Manual*, Eaton, Canada, 2013.

[5] P. C. Chiu et al., Compensation strategies for ramping waveform of TPS booster synchrotron main power supplies, *Proc. of the 6th International Particle Accelerator Conference*, Richmond, VA, USA, pp.1088-1090, 2015.

[6] K. B. Liu, Y. D. Li, B. S. Wang, K. T. Hsu and J. C. Hsu, TPS corrector magnet power converter, *Proc. of the 1st International Particle Accelerator Conference*, Kyoto, Japan, pp.3269-3271, 2010.

[7] N. Mohan, T. Undeland and W. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd Edition, John Willey&Sons Inc., USA, 2003.

[8] K. J. Åström and T. Hägglund, *Advanced PID Control*, International Society of Automation, 2006.

[9] D. A. Bristow, M. Tharayil and A. G. Alleyne, A survey of iterative learning control, *IEEE Control Systems Magazine*, vol.26, no.3, pp.96-114, 2006.

[10] Y. Wang, F. Gao and F. R. D. III, Survey on iterative learning control, repetitive control, and run-to-run control, *Journal of Process Control*, vol.19, no.10, pp.1589-1600, 2009.

[11] L. Ben-Brahim, M. Benammar and M. A. Alhamad, New iterative learning control method for PWM inverter current regulation, *IEEE Trans. Power Electronics*, vol.2, pp.1460-1465, 2003.

[12] W. Wei, S. K. Panda and J. X. Xu, Control of high performance DCAC inverters using iterative learning control, *IEEE Trans. Power Electronics*, vol.4, pp.132-135, 2004.

[13] Y. Q. Wang and F. J. D. III, Stability analysis for set-pointrelated indirect iterative learning control, *Proc. of the 48th IEEE Conference on Decision and Control*, pp.5702-5707, 2009.